Calculate EC-BIT Thresholds on CoherentDSP Controllers

Contents

Introduction

This document describes how to calculate and configure ec-bits thresholds on coherentDSP controllers.

Prerequisites

Cisco recommends familiarity with optical networking terminology and the Network Convergence System 1000 series.

Background Information

An ec-bit or error-corrected bit represents a single bit error received on a coherentDSP controller. Forward Error Correction (FEC) automatically corrects errored bits within the maximum Bit Error Ratio (BER) threshold listed in the table. For other Cisco equipment with coherentDSP controllers, refer to the product documentation for the BER threshold.

Product ID	Modulation Type	FEC Type	Pre-FEC BER Threshold
ONS-CFP2-WDM	QPSK (100G)	7% SoftDecision	1.0E-2
ONS-CFP2-WDM	QPSK (100G)	20% SoftDecision	3.6E-2
ONS-CFP2-WDM	16-QAM (200G & 250G)	7% SoftDecision	0.75E-2
ONS-CFP2-WDM	16-QAM (200G & 250G)	20% SoftDecision	2.4E-2
NCS1K4-1.2T-K9	all	15% SoftDecision	2.0E-2
NCS1K4-1.2T-K9	all	27% SoftDecision	3.75E-2

Source

Table 4. https://www.cisco.com/c/en/us/products/collateral/optical-networking/network-convergence-system-1000...

Table 6. https://www.cisco.com/c/en/us/products/collateral/optical-networking/network-convergence-system-1000...

Errored bits in excess of the maximum Bit Error Ratio (BER) are not corrected and increment as Post-FEC errors. Depending on configuration, Post-FEC errors can pass on to the client or result in a client port squelch.

Squelch disables transmission from client interfaces for the duration of the trunk error. Configuration of the ec-bits threshold enables proactive detection of signal degradation before Post-FEC errors increment.

This configuration does not predict or protect against bursts of uncorrected words.

You can view the current BER of a coherentDSP controller with **show controller coherentDSP 0/0/0/x**.

```
RP/0/RP0/CPU0:NCS1002_1# show controller coherentDSP 0/0/0/5
Tue Jul 18 14:54:19.399 UTC

Port : CoherentDSP 0/0/0/5
Controller State : Up
Inherited Secondary State : Normal
Configured Secondary State : Normal
Derived State : In Service
Loopback mode : None
BER Thresholds : SF = 1.0E-5 SD = 1.0E-7
Performance Monitoring : Enable

Alarm Information:
LOS = 6 LOF = 3 LOM = 1
OOF = 3 OOM = 4 AIS = 0
IAE = 0 BIAE = 0 SF_BER = 0
SD_BER = 0 BDI = 6 TIM = 0
FECMISMATCH = 0 FEC-UNC = 1
Detected Alarms : None

Bit Error Rate Information
PREFEC BER : 5.8E-03
POSTFEC BER : 0.0E+00

TTI :
Remote hostname : NCS1002_2
Remote interface : CoherentDSP 0/0/0/5
Remote IP addr : 0.0.0.0

FEC mode : Soft-Decision 20

AINS Soak : None
AINS Timer : 0h, 0m
AINS remaining time : 0 seconds
```

Requirements

This configuration requires a device with coherentDSP controllers such as the NCS1002 or NCS1004.

Components Used

This example uses:

- NCS1002 on XR 7.3.2 with ONS-CFP2-WDM pluggables configured in 200G slice mode.
- NCS1004 on XR 7.9.1 with the NCS1K4-1.2T-K9 configured in 400G mxponder mode.

The information in this document was created from the devices in a specific lab environment. All of the devices used in this document started with a cleared (default) configuration. If your network is live, ensure that you understand the potential impact of any command.

Configure

The 30-second, 15-minute, and 24-hour Performance Monitoring (PM) intervals can all have an ec-bits thresholds.

1. Determine the bit rate of the coherentDSP controller for each PM interval.

The trunk rate appears in various locations depending on the platform. The NCS1002 lists the trunk rate under **show hw-module slice *x***

```
<#root>

RP/0/RP0/CPU0:NCS1002_1#

show hw-module slice 0

Tue Jul 18 15:42:17.725 UTC
Slice ID: 0
Status: Provisioned
Client Bitrate: 100
Trunk Bitrate: 200
DP FPGA FW Type: X100
DP FPGA FW Version: 01.01
HW Status: CURRENT
```

The NCS1004 gives the bandwidth under **show controller coherent 0/x/0/y**.

```
<#root>

RP/0/RP0/CPU0:NCS1004_71#

show controller coherentDSP 0/1/0/0

Tue Jul 18 12:10:59.777 CDT

Port : CoherentDSP 0/1/0/0
Controller State : Up
Inherited Secondary State : Normal
Configured Secondary State : Normal
Derived State : In Service
Loopback mode : None
BER Thresholds : SF = 1.0E-5 SD = 1.0E-7
Performance Monitoring : Enable
Bandwidth : 400.0Gb/s

Alarm Information:
LOS = 1 LOF = 1 LOM = 0
```

```
OOF = 1 OOM = 1 AIS = 0
IAE = 0 BIAE = 0 SF_BER = 0
SD_BER = 0 BDI = 0 TIM = 0
FECMISMATCH = 0 FEC-UNC = 0 FLEXO_GIDM = 0
FLEXO-MM = 0 FLEXO-LOM = 0 FLEXO-RDI = 0
FLEXO-LOF = 0
Detected Alarms : None

Bit Error Rate Information
PREFEC BER : 8.78E-04
POSTFEC BER : 0.00E+00
Q-Factor : 9.80 dB

Q-Margin : 4.80dB

Instantaneous Q-Margin : 4.50 dB
```

A 200 Gbps bit rate gives these number of bits for each PM interval.

- 30-sec: 2E11 bits/second * 30 seconds = 6E12 bits
- 15-min: 2E11 bits/second * 60 seconds * 15 minutes = 1.8E14 bits
- 24-hour: 2E11 bits/second * 60 seconds * 60 minutes * 24 hours = 1.728E16 bits

A 400 Gbps bit rate gives double these rates:

- 30-sec: 4E11 bits/second * 30 seconds = 1.2E13 bits
- 15-min: 4E11 bits/second * 60 seconds * 15 minutes = 3.6E14 bits
- 24-hour: 4E11 bits/second * 60 seconds * 60 minutes * 24 hours = 3.46E16 bits

2. Calculate the maximum allowable threshold of error-corrected bits per interval. Repeat these steps for the 15-minute interval. Because the 24-hour threshold has limited usefulness, you do not need to calculate it.

Example 1: A 200G signal using 20% SoftDecision (SD) FEC has a maximum pre-FEC BER of 2.4E-2 from the table.

- 30-sec: 6E12 bits * 2.4E-2 BER = 1.44E11 ec-bits = 144000000000 ec-bits
- 15-min: 1.8E14 bits * 2.4E-2 BER = 4.32E12 ec-bits = 4320000000000 ec-bits

Example 2: A 400G signal using 27% SD FEC has a maximum pre-FEC BER tolerance of 3.75E-2.

- 30-sec: 1.2E13 bits * 3.75E-2 = 4.5E11 = 450000000000 ec-bits
- 15-min: 3.6E14 bits * 3.75E-2 = 1.35E13 = 13500000000000 ec-bits

In general, configure the ec-bit threshold between the current BER and the maximum tolerance.

For example, a 400G coherentDSP controller could report an average BER of 8.83E-4, giving a total of 10596000000 errored bits in one 30 second interval.

To prevent unnecessary threshold crossing alerts (TCAs) in **show logging**, set the threshold greater than this value.

This example sets the threshold within about 20% of the maximum tolerance of errored bits.

3. Configure the ec-bits threshold on the coherentDSP controller.

Example 1: NCS1002 with 200G trunk rate using 20% SoftDecision FEC.

```
<#root>

RP/0/RP0/CPU0:NCS1002_1#

configure

Tue Jul 18 17:22:14.088 UTC
RP/0/RP0/CPU0:NCS1002_1(config)#

controller coherentDSP 0/0/0/5

RP/0/RP0/CPU0:NCS1002_1(config-CoDSP)#

pm 30-sec fec threshold ec-bits 115200000000

RP/0/RP0/CPU0:NCS1002_1(config-CoDSP)#

pm 15-min fec threshold ec-bits 3456000000000

RP/0/RP0/CPU0:NCS1002_1(config-CoDSP)#

commit
```

Example 2: NCS1004 with the NCS1K4-1.2T-K9 using 400G mxponder mode with 27% SoftDecision FEC.

```
<#root>

RP/0/RP0/CPU0:NCS1004_1#

configure

Tue Jul 18 11:52:17.915 CDT
RP/0/RP0/CPU0:NCS1004_1(config)#

controller coherentDSP 0/1/0/0

RP/0/RP0/CPU0:NCS1004_1(config-CoDSP)#

pm 30-sec fec threshold ec-bits 360000000000

RP/0/RP0/CPU0:NCS1004_1(config-CoDSP)#

pm 15-min fec threshold ec-bits 10800000000000

RP/0/RP0/CPU0:NCS1004_1(config-CoDSP)#

commit
```

Repeat these steps for all coherentDSP controllers in service including the far end devices.

Network Diagram

NCS1002_1 0/0/0/5 <----> 0/0/0/5 NCS1002_2

NCS1004_1 0/1/0/0 <----> 0/1/0/0 NCS1004_1

Configurations

To disable reporting of all TCAs for ec-bits, use the commands:

```
<#root>

RP/0/RP0/CPU0:NCS1004_1(config-CoDSP)#

 pm 30-sec fec report ec-bits disable

RP/0/RP0/CPU0:NCS1004_1(config-CoDSP)#

 pm 15-min fec report ec-bits disable

RP/0/RP0/CPU0:NCS1004_1(config-CoDSP)#

pm 24-hour fec report ec-bits disable

RP/0/RP0/CPU0:NCS1004_1(config-CoDSP)#

commit
```

Verify

Verify the changes took effect with **show run controller coherentDSP 0/x/0/y**.

```
<#root>

RP/0/RP0/CPU0:NCS1002_1#

show run controller coherentDSP 0/0/0/5

Tue Jul 18 17:47:03.392 UTC
controller CoherentDSP0/0/0/5
 pm 15-min fec threshold ec-bits 3800000000000
 pm 30-sec fec threshold ec-bits 130000000000
!
```

```
<#root>

RP/0/RP0/CPU0:NCS1004_1#

show run controller coherentDSP 0/1/0/0

Tue Jul 18 12:39:46.782 CDT
controller CoherentDSP0/1/0/0
 pm 15-min fec threshold ec-bits 12000000000000
 pm 30-sec fec threshold ec-bits 400000000000
!
```