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1.1 ots 0.5.0

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1.2 mksh 57

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RCSID: $MirOS: src/bin/mksh/mksh.faq,v 1.6 2020/04/13 20:46:39 tg Exp $
ToC: spelling
Title: How do you spell <tt>mksh</tt>? How do you pronounce it?

<p>This shell is spelt either
"<tt>mksh</tt>" (with, even at the beginning of a sentence, <a
href="https://en.wikipedia.org/wiki/Wikipedia:Manual_of_Style/Capital_letters#Items_that_require_initial_lower_c
ase">an
initial lowercase letter; this is important) or "MirBSD Korn Shell",
possibly with "the".</p>
<p>I usually pronounce it as "em-ka-es-ha",
that is, the letters individually in my native German, or say "MirBSD Korn
Shell", although it is manageable, mostly for Slavic speakers, to actually
say "mksh" as if it were a word </p>
<p>Oh… I've run into this one, didn't I? "MirBSD" is pronounced "Mir-Be-Es-De" germanically, for anglophones
"Mir-beas'tie" is fine.</p>

ToC: sowhatismksh
Title: I'm a $OS (<i>Android, OS/2, …</i>) user, so what's mksh?

<p>mksh is a so-called (Unix) "shell" or "command interpreter", similar to
<tt>COMMAND.COM</tt>, <tt>CMD.EXE</tt> or PowerShell on other operating
systems you might know. Basically, it runs in a terminal ("console" or
"DOS box") window, taking user input and running that as commands. It's
also used to write so-called (shell) "script"s, short programs made by
putting several of those commands into a "batch file".</p>
<p>On Android, mksh is used as the system shell—basically, the one
running commands at system startup, in the background, and on user
behalf (but never of its own). Any privilege pop-ups you might <a
href="https://forum.xda-developers.com/showthread.php?t=1963976">be
encountering are therefore <a
href="https://forum.xda-developers.com/showpost.php?p=33550523&postcount=1553">not
caused by mksh but by some other code invoking mksh to do something
on its behalf.</p>

ToC: os2
Title: I'm an OS/2 user, what else do I need to know?

<p>Unlike the native command prompt, the current working directory is,
for security reasons common on Unix systems which the shell is designed
for, not in the search path at all; if you really need this, run the
command <tt>PATH=.$PATHSEP$PATH</tt> or add that to a suitable
initialisation file (<tt>~/.mkshrc</tt>).</p>
<p>There are two different newline modes for mksh-os2: standard (Unix)
mode, in which only LF (0A hex) is supported as line separator, and
"textmode", which also accepts ASCII newlines (CR+LF), like most other
tools on OS/2, but creating an incompatibility with standard mksh. If
you compiled mksh from source, you will get the standard Unix mode unless
<tt>-T</tt> is added during compilation; however, you will most likely
have gotten this shell through komh's port on Hobbes, or from his OS/2
Factory on eComStation Korea, which uses "textmode", though. Most OS/2
users will want to use "textmode" unless they need absolute compatibility
with Unix mksh and other Unix shells and tools.</p>

ToC: kornshell
Title: How does this relate to ksh or the Korn Shell?

<p>The Korn Shell (AT&T ksh) was authored by David Korn; two major
flavours exist (ksh88 and ksh93), the latter having been maintained
until 2012 (last formal release) and 2014 (last beta snapshot, buggy).
A ksh86 did exist.</p>
<p>There's now <tt>ksh2020</tt>, a project having restarted development
around November 2017 forking the last <tt>ksh93 v-</tt> (beta) snapshot
and continuing to develop it, presented at FOSDEM.</p>
<p>AT&T ksh88 is "the (original) Korn Shell". Other implementations,
of varying quality (MKS Toolkit's MKS ksh being named as an example of
the lower end, MirBSD's mksh at the upper end). They are all not
"Korn Shell" or "ksh". However, mksh got blessed by David Korn, as long
as it cannot be confused with the original Korn Shell.</p>
<p>The POSIX shell standard, while lacking most Korn Shell features, was
largely based on AT&T ksh88, with some from the Bourne shell.</p>
<p>mksh is the currently active development of what started as the Public
Domain Bourne Shell in the mid-1980s with ksh88-compatibl-ish extensions
having been added later, making the Public Domain Korn Shell (pdksh),
which, while never officially blessed, was the only way for most to get
a Korn Shell-like command interpreter for AT&T's was proprietary,
closed-source code for a very long time. pdksh's development ended in
1999, with some projects like Debian and NetBSD® creating small bug fixes
(which often introduced new bugs) as part of maintenance. Around 2003,
OpenBSD started cleaning up their shipped version of pdksh, removing old
and compatibility code and modernising it. In 2002, development of what
is now mksh started as the system shell of MirBSD, which took over almost
all of OpenBSD's cleanup, adding compatibility to other operating systems
back on top of it, and after 2004, independent, massive development of
bugfixes including a complete reorganisation of the way the parser works,
and of new features both independent and compatible with other shells

(ksh93, GNU bash, zsh, BSD csh) started and was followed by working with
the group behind POSIX to fix issues both in the standard and in mksh.
mksh became the system shell in several other operating systems and Linux
distributions and Android and thus is likely the Korn shell, if not Unix
shell, flavour with the largest user base. It has replaced pdksh in all
contemporary systems except QNX, NetBSD® and OpenBSD (who continue to
maintain their variant on "low flame").</p>
<p>dtksh is the "Desktop Korn Shell", a build of AT&T ksh93 with some
additional built-in utilities for graphics programming (windows, menu
bars, dialogue boxes, etc.) utilising Motif bindings.</p>
<p>MKS ksh is a proprietary reimplemention aiming for, but not quite
getting close to, ksh88 compatibility.</p>
<p>SKsh is an AmigaOS-specific Korn Shell-lookalike by Steve Koren.</p>
<p>The Homepage of the <tt>#ksh</tt>
channel on Freenode IRC contains more information about the Korn
Shell in general and its flavours.</p>

ToC: packaging
Title: How should I package mksh? (common cases)

<p>Export a few environment variables, namely <tt>CC</tt> (the C compiler),
<tt>CPPFLAGS</tt> (all C præprocessor definitions), <tt>CFLAGS</tt> (only
compiler flags, no <tt>-Dfoo</tt> or anything!), <tt>LDFLAGS</tt>
(for anything to pass to the C compiler while linking) and <tt>LIBS</tt>
(appended to the linking command line after everything else. You might
wish to <tt>export LDSTATIC=-static</tt> for a static build as well.</p>
<p>When cross-compiling, <tt>CC</tt> is the cross compiler (mksh
currently does not require a compiler targetting the build system), but
you must also export <tt>TARGET_OS</tt> to whatever system you
are compiling for, e.g. "Linux". For most operating systems, that's just
the uname(1) output. Some very rare systems also need <tt>TARGET_OSREV</tt>;
consult the source code of <tt>Build.sh</tt> for details.</p>
<p>Create two subdirectories, say <tt>build-mksh</tt> and <tt>build-lksh</tt>.
In each of them, start a compilation by issuing <tt>sh ../Build.sh -r</tt>
followed by running the testsuite[1] via
<tt>./test.sh</tt>. For lksh(1) add <tt>-DMKSH_BINSHPOSIX</tt> to
<tt>CPPFLAGS</tt> and use <tt>sh ../Build.sh -r -L</tt> to compile.</p>
<p>See below if the testsuite fails.</p>
<p>Install <tt>build-mksh/mksh</tt> as <tt>/bin/mksh</tt> (or similar),
<tt>build-lksh/lksh</tt> as <tt>/bin/lksh</tt> with a symlink(7) to it
from <tt>/bin/sh</tt> (if desred), and <tt>mksh.1</tt> and <tt>lksh.1</tt>
as manpages (mdoc macropackage required). Install <tt>dot.mkshrc</tt>
either as <tt>/etc/skel/.mkshrc</tt> (meaning your users will have to
manually resynchronise their home directories' copies after every package
upgrade) or as <tt>/etc/mkshrc</tt>, in which case you install a <a
href="https://evolvis.org/plugins/scmgit/cgi-
bin/gitweb.cgi?p=alioth/mksh.git;a=blob;f=debian/.mkshrc;hb=HEAD">redirection
script like Debian's into <tt>/etc/skel/.mkshrc</tt>. You may need a <a

href="@@RELPATH@@TaC-mksh.txt">summary of the licence information.</p>
<p>At runtime, the presence of <tt>/bin/ed</tt> as default history editor
is recommended, as well as a manpage formatter; you can also install
preformatted manpages from <tt>build-*ksh/*ksh.cat1</tt> if nroff(1) (or
<tt>$NROFF</tt>) is available at build time by removing the <tt>-r</tt>
flag from either <tt>Build.sh</tt> invocation.</p>
<p>Some shell features require the ability to create temporary files and
FIFOS (cf. mkfifo(2))/pipes at runtime. Set <tt>TMPDIR</tt> to a suitable
location if <tt>/tmp</tt> isn't it; if this is known ahead of time, you
can add <tt>-DMKSH_DEFAULT_TMPDIR=\"/path/to/tmp\"</tt> to CPPFLAGS. We
currently are unable to determine one on Android because its bionic libc
does not expose any method suitable to do so in the generic case.</p>
<p id="packaging-fn1"> To run the testsuite, ed(1) must be available as
<tt>/bin/ed</tt>, and perl(1) is needed. When cross-compiling, the version
of the first <tt>ed</tt> binary on the <tt>PATH</tt> must be the
same as that in the target system on which the tests are to be run, in
order to be able to detect which flavour of ed to adjust the tests for.
Busybox ed is broken beyond repair, and all three ed-related tests will
always fail with it.</p>

ToC: mkshrc
Title: How does mksh load configuration files?

<p>The shell loads first <tt>/etc/profile</tt> then <tt>~/.profile</tt>
if called as login shell or with the <tt>-l</tt> flag, then loads the file
<tt>$ENV</tt> points to (defaulting to <tt>~/.mkshrc</tt>) for interactive
shells (that includes login shells).</p>
<p>Distributors should take care to either install the <tt>dot.mkshrc</tt>
example provided into <tt>/etc/skel/.mkshrc</tt> (so that it's available
for newly created user accounts) and ensure it can propagate to existing
accounts or, if upgrading these is difficult, install the shipped file
as, for example, <tt>/etc/mkshrc</tt> and install a skeleton file, such
as the one in Debian, that sources the file in <tt>/etc</tt>.</p>
<p>It's vital that users can change the configuration, so do not force a
root-provided config file onto them; the shipped file, after all, is just
an example.</p>
<p>If you need central user and configuration management and cannot use
something that installs skeleton files upon home directory creation
(like pam_mkhomedir), you can <tt>export ENV</tt> in <tt>/etc/profile</tt>
to a file (say <tt>/etc/shellrc</tt>) that sources the per-shell file.
Users can, this way, still override it by setting a different <tt>$ENV</tt>
in their <tt>~/.profile</tt>.</p>

ToC: testsuite-fails
Title: The testsuite fails!

<p>The mksh testsuite has uncovered numerous bugs in operating systems
(kernels, libraries), compilers and toolchains. It is likely that you

just ran into one. If you're using LTO (the <tt>Build.sh</tt> option
<tt>-c lto</tt>) try to disable it first—especially GCC is a repeat
offender breaking LTO and its antecessor <tt>-fwhole-program --combine</tt>
and tends to do wrong code generation quite a bit. Otherwise, try
lowering the optimisation levels, bisecting, etc.</p>

ToC: selinux-androidiocy

Title: I forbid stat(2) in my SELinux policy, and some things do not work!

Don't break Unix. Read up on the GIGO principle. Duh.

ToC: makefile

Title: Why doesn't this use a Makefile to build?

<p>Not all supported target operating environments have a make utility
available, and shell was required for "mirtoconf" (like autoconf)
already anyway, so it was chosen to run the make part as well.</p>
<p>You can, however, add the <tt>-M</tt> flag to your <tt>Build.sh</tt>
invocations to let it produce a <tt>Makefrag.inc</tt> file tailored
for this specific build which you can then include in a Makefile,
such as with the BSD make(1) ".include" command or <a
href="https://www.gnu.org/software/make/manual/make.html#Include">GNU
make equivalent. It even contains, for the user to start out with,
a commented-out example of how to do that in the most basic manner.</p>

ToC: oldbsd

Title: Why do other BSDs and QNX still use pdksh instead of mksh?

<p>Some systems are resistent to change, mostly due to bikeshedding
(some people would, for example, rather see all shells banned to
ports/pkgsrc®) and hysterial raisins (historical reasons). Most
BSDs have mksh packages available, and it works on all of them and
QNX just fine.</p>
<p>In fact, on all of these systems, you can replace their 1999-era
<tt>/bin/ksh</tt> (which is a pdksh) with mksh. On at least NetBSD®
1.6 and up (not 1.5) and OpenBSD, even <tt>/bin/sh</tt> is fair game.</p>
<p>MidnightBSD notably has adopted mksh as system shell (thanks laffer1).</p>

ToC: openbsd

Title: Why is there no mksh in OpenBSD's ports tree?

OpenBSD don't like people who fork off their project at all; heck,
they don't even like the people they themselves forked off (NetBSD®).
Several people tried over the years to get one committed, but nobody
dared so as to not lose their commit bit. If you try, succeed, and
survive Theo, however, kudos to you! See also the
"other BSDs" FAQ entry.

ToC: book
Title: I'd like an introduction.

Unfortunately, nobody has written a book about mksh yet, although
other shells have received (sometimes decent) attention from authors
and publishers. This FAQ lists a subset of things packagers and
generic people ask, and the mksh(1) manpage is more of a reference,
so you are probably best off starting with a shell-agnostic, POSIX
or ksh88 reference such as the first edition (the second one deals
with ksh93 which differs far more from mksh than ksh88, as ancient
as it is, does) of the O'Reilly book (disclaimer: only an example,
not a recommendation) and going forward by reading scripts (the
"shellsnippets" repository referenced in the <tt>#ksh</tt> channel
homepage (see the top of this document) has many examples) and
trying to understand them and the mksh specifics from the manpage.

ToC: ps1conv
Title: My prompt from <<i>some other shell</i>> does not work!

Contact us on the mailing list or on IRC,
we'll convert it for you. Also have a look at the PS1 section in
the mksh(1) manpage (search for "otherwise unused char", e.g. with
<tt>/</tt> in less(1), to spot it quickly).

ToC: ps1weird
Title: My prompt is weird!

<p>There are several reasons why your <tt>PS1</tt> might be not
what you'd expect:</p>
<tt>$PS1</tt> is <tt>export</tt>ed. Do not export PS1!
(This was agreed upon as suggestion in a discussion between bash, zsh and
Korn shell developers.) The feature set of different shells vastly differs
and each shell should use its default PS1 or from its startup files.
<tt>$ENV</tt> is set and/or <tt>export</tt>ed.
Your prompt is just "<tt># </tt>": you're entering a root shell, and
<tt>$PS1</tt> does not contain the '#' character, in which case the shell
forces this prompt, making extra privileges obvious.
Your prompt is just "<tt>$ </tt>": perhaps your system administrator
did not install the shipped <tt>dot.mkshrc</tt> file, or you did not copy
<tt>/etc/skel/.mkshrc</tt> into your home directory (perhaps it was created
before <tt>mksh</tt> was installed?). Without another idea for a fix, get <a
href="http://www.mirbsd.org/cvs.cgi/~checkout~/src/bin/mksh/dot.mkshrc?rev=HEAD;content-
type=text%2Fplain">this
file and store it as <tt>~/.mkshrc</tt> then run <tt>mksh</tt>; this
will at the very least install our sample ("user@host:path $ ") prompt.
Your prompt contains things like "\u" or "\w": it is for another shell
and needs converting.
Your prompt contains colours, and when the command line is long the

cursor position or screen contents, especially using the history, is off:
terminal escapes must be escaped from the shell; check the PS1 section in
the manpage: search for "otherwise unused char" (see above).
If the prompt doesn't leave enough space on the right, the shell inserts
a line break after it when rendering.

ToC: env
Title: On startup files and <tt>$ENV</tt> across and detecting various shells

Interactive shells look at <tt>~/.mkshrc</tt> (or <tt>/system/etc/mkshrc</tt>
on Android and <tt>/etc/mkshrc</tt> on FreeWRT and OpenWrt) by default. This
location can, however, be overridden by setting the <tt>ENV</tt> environment
variable. (FreeBSD is rumoured to set it in their system profile.) It's better
to not set <tt>$ENV</tt> if possible and let every shell user their native
startup files; otherwise, you must ensure that it runs under all shells. Check
<tt>$BASH_VERSION</tt> (GNU bash), <tt>$KSH_VERSION</tt> (contains "LEGACY KSH"
or "MIRBSD KSH" for mksh, "PD KSH" for ancient mirbsdksh/oksh/pdksh, "Version"
for ksh93); <tt>$NETBSD_SHELL</tt> (NetBSD ash); <tt>POSH_VERSION</tt> (posh, a
pdksh derivative); <tt>$SH_VERSION</tt> ("PD KSH" as sh), <tt>$YASH_VERSION</tt>
(yash), <tt>$ZSH_VERSION</tt> (or if <tt>$VERSION</tt> begins with "zsh"); a <a
href="@@RELPATH@@ksh-chan.htm#which-shell">list of more approaches exists.

ToC: ctrl-l-cls
Title: ^L (Ctrl-L) does not clear the screen

Use ^[^L (Escape+Ctrl-L) or rebind it:
<tt>bind '^L=clear-screen'</tt>

ToC: ctrl-u-pico
Title: ^U (Ctrl-U) clears the entire line

If it should only delete the line up to the cursor, use:
<tt>bind -m ^U='^[0^K'</tt>

ToC: cur-up-zsh
Title: Cursor Up behaves differently from zsh

Some shells make Cursor Up search in the history only for commands
starting with what was already entered. mksh separates the shortcuts:
Cursor Up goes up one command and PgUp searches the history as described
above. You can, of course, rebind:
<tt>bind '^XA=search-history-up'</tt>

ToC: current
Title: Can mksh set the title of the window according to the command running?

There's no such thing as "the command currently running"; consider

pipelines and delays (<tt>cmd1 | (cmd2; sleep 3; cmd3) | cmd4</tt>).
There is, however, a way to make the shell display the command line
during the time it is executed; for testing, you will need to download <a
href="https://evolvis.org/plugins/scmgit/cgi-
bin/gitweb.cgi?p=shellsnippets/shellsnippets.git;a=blob;f=mksh/terminal-title;hb=HEAD">this
script and <tt>source</tt> it. For merging into your <tt>~/.mkshrc</tt>
you should first understand how it works: lines 4–18 set a <tt>PS1</tt>
(prompt) equivalent to lines 84–96 of the stock <tt>dot.mkshrc</tt>, with
one change: line 15 (<tt>print >/dev/tty …</tt>) is new, inserted just
before the <tt>return</tt> command of the function substitution in the
default prompt; this is what you'll need to merge into your own, custom,
prompt (if you have one; otherwise pull this adaption to the default
one). Line 19 is the only other thing in this script rebinding the Ctrl-M
key (which is normally produced by the Enter/Return key) to code that…
does something crazy. This trick however does funny things with
multiline commands, so if you type something out in multiple lines,
for example here documents or loops press
Ctrl-J instead of Enter/Return after each line
including the first (at PS1) and final (at PS2) one.

ToC: other-tty
Title: How do I start mksh on a specific terminal?

<p>Normally: <tt>mksh -T<i>/dev/tty2</i></tt></p>
<p>However, if you want for it to return (e.g. for an embedded system rescue
shell), use this on your real console device instead:
<tt>mksh -T!<i>/dev/ttyACM0</i></tt></p>
<p>mksh can also daemonise (send to the background):
<tt>mksh -T- -c 'exec cdio lock'</tt></p>

ToC: completion
Title: What about programmable tab completion?

The shell itself provides static deterministic tab completion.
However, you can use hooks like reprogramming the Tab key to a
command line editor macro, and using the <tt>evaluate-region</tt>
editor command (modulo a bugfix) together with <tt>quote-region<tt> and shell functions to
implement a programmable completion engine. Multiple people have
been considering doing so in our IRC channel; we'll hyperlink to
these engines when they are available.

ToC: posix-mode
Title: How POSIX compliant is mksh? Also, UTF-8 vs. locales?

<p>You'll need to use the <tt>lksh</tt> binary, unless your C <tt>long</tt>
type is 32 bits wide, for POSIX-compliant arithmetic in the shell. This is
because <tt>mksh</tt> provides consistent, wraparound-defined, 32-bit
arithmetics on all platforms normally. You'll also need to enable POSIX mode

(<tt>set -o posix</tt>) explicitly, which also disables brace expansion upon
being enabled (use <tt>set -o braceexpand</tt> to reenable if needed).</p>
<p>For the purpose of POSIX, mksh supports only the <tt>C</tt> locale. mksh's
<tt>utf8-mode</tt> (which only supports the BMP (Basic Multilingual Plane) of
UCS and maps raw octets into the U+EF80U+EFFF wide character range; see
<tt>Arithmetic expressions</tt> in mksh(1) for details) must stay
disabled in POSIX mode (it is disabled upon enabling POSIX mode in R56+).</p>
<p class="boxhead">The following POSIX sh-compatible code toggles the
<tt>utf8-mode</tt> option dependent on the current POSIX locale, for mksh
to allow using the UTF-8 mode, within the constraints outlined above, in
code portable across various shell implementations:</p>
<div class="boxtext">
<pre>
 case ${KSH_VERSION:-} in
 MIRBSD KSH|*LEGACY KSH*)
 case ${LC_ALL:-${LC_CTYPE:-${LANG:-}}} in
 [Uu][Tt][Ff]8|*[Uu][Tt][Ff]-8*) set -U ;;
 *) set +U ;;
 esac ;;
 esac
</pre>
</div><p class="boxfoot">In near future, (UTF-8) locale tracking will
be implemented, though.</p>
<p>The shell is pretty close to POSIX, when run as <tt>lksh -o posix</tt>
under the "C" locale it is intended to match. It does not do everything
like other POSIX-compatible or compliant shells, though.</p>

ToC: function-local-scopes
Title: What differences in function-local scopes are there?

<p><tt>mksh</tt> has a different scope model from AT&T <tt>ksh</tt>,
which leads to subtle differences in semantics for identical builtins.
This can cause issues with a <tt>nameref</tt> to suddenly point to a
local variable by accident. (Other common shells share mksh's scoping
model.)</p>
<p class="boxhead">GNU <tt>bash</tt> allows unsetting local variables; in
<tt>mksh</tt>, doing so in a function allows back access to the global
variable (actually the one in the next scope up) with the same name. The
following code, when run before function definitions, changes the behaviour
of <tt>unset</tt> to behave like other shells (the alias can be removed
after the definitions):</p>
<div class="boxtext">
<pre>
 case ${KSH_VERSION:-} in
 MIRBSD KSH|*LEGACY KSH*)
 function unset_compat {
  \\builtin typeset unset_compat_x

```
  for unset_compat_x in "$@"; do
   eval "\\\\builtin unset $unset_compat_x[*]"
  done
  }
 \\builtin alias unset=unset_compat
 ;;
 esac
</pre>
</div><p class="boxfoot">When a local variable is created (e.g. using
<tt>local</tt>, <tt>typeset</tt>, <tt>integer</tt> or
<tt>\\builtin typeset</tt>) it does not, like in other shells, inherit
the value from the global (next scope up) variable with the same name;
it is rather created without any value (unset but defined).</p>
----
ToC: regex-comparison
Title: I get an error in this regex comparison

<p>Use extglobs instead of regexes:<br />
<tt>[[ foo =~ (foo|bar).*baz ]]</tt><br />
… becomes…<br />
<tt>[[ foo = *@(foo|bar)*baz* ]]</tt></p>
----
ToC: extensions-to-avoid
Title: Are there any extensions to avoid?

<p>GNU <tt>bash</tt> supports "<tt>&amp;&gt;</tt>" (and "|&amp;") to redirect
both stdout and stderr in one go, but this breaks POSIX and Korn Shell syntax;
use POSIX redirections instead:</p>
<table border="1" cellpadding="3">
<tr><td>GNU bash</td><td>
 <tt>foo |&amp; bar |&amp; baz &amp;&gt;log</tt>
</td></tr>
<tr><td>POSIX</td><td>
 <tt>foo 2&gt;&amp;1 | bar 2&gt;&amp;1 | baz &gt;log 2&gt;&amp;1</tt>
</td></tr>
</table>
----
ToC: while-read-pipe
Title: Something is going wrong with my while...read loop

<p class="boxhead">Most likely, you've encountered the problem in which
the shell runs all parts of a pipeline as subshell. The inner loop will
be executed in a subshell and variable changes cannot be propagated if
run in a pipeline:</p>
<div class="boxtext">
<pre>
 bar | baz | while read foo; do ...; done
</pre>
```

</div><p class="boxfoot">Note that <tt>exit</tt> in the inner loop will also only exit the subshell and not the original shell. Likewise, if the code is inside a function, <tt>return</tt> in the inner loop will only exit the subshell and won't terminate the function.</p>
<p class="boxhead">Use co-processes instead:</p>
<div class="boxtext">
<pre>
 bar | baz |&
 while read -p foo; do ...; done
 exec 3>&p; exec 3>&-
</pre>
</div><p class="boxfoot">If <tt>read</tt> is run in a way such as <tt>while read foo; do ...; done</tt> then leading whitespace will be removed (IFS) and backslashes processed. You might want to use <tt>while IFS= read -r foo; do ...; done</tt> for pristine I/O.</p>
<p class="boxhead">Similarly, when using the <tt>-a</tt> option, use of the <tt>-r</tt> option might be prudent (<tt>read -raN-1 arr <file</tt>); the same applies for NUL-terminated lines:</p>
<div class="boxtext">
<pre>
 find . -type f -print0 |& \
    while IFS= read -d " -pr filename; do
  print -r -- "found <${filename#./}>"
 done
</pre>
</div>

ToC: command-alias
Title: "command" doesn't expand aliases as in ksh93

This is because AT&T ksh93 ships a predefined alias enabling this:
<tt>alias command='command '</tt>
put this into your <tt>~/.mkshrc</tt>
(note the space before the closing single quote)

ToC: builtin-rename
Title: "rename" doesn't work as expected!

<p>There's a <tt>rename</tt> built-in utility in mksh, which is a very thin wrapper around the rename(2) syscall. It receives two pathnames, source and destination where the first is then atomically renamed to the latter. It does not move, i.e. fails for different filesystems.</p>
<p>The GNU package <tt>util-linux</tt> has a different <tt>rename</tt> command. If you wish to invoke an external utility (in favour over a builtin), you can use <tt>dot.mkshrc</tt>'s function <tt>enable</tt> or put the following into your <tt>~/.mkshrc</tt>:</p>
<pre>alias rename="$(whence -p rename)"</pre>

ToC: builtin-sleep

Title: "sleep" does not accept 'm' for minutes!

<p>mksh contains a <tt>sleep</tt> built-in utility, in order to be
able to offer sub-second sleep to shell scripts for most platforms.
(It does not exist if the platform lacks select(2)—which should
be rare.)</p>
<p>GNU coreutils contains a sleep implementation accepting suffixed
numbers. If you wish to invoke an external utility (in favour over a
builtin), you can use <tt>dot.mkshrc</tt>'s function <tt>enable</tt>
or put something along the following lines into <tt>~/.mkshrc</tt>:</p>
<pre>alias sleep="$(whence -p sleep)"</pre>
<pre>timer() { sleep $(($1*60${2:++$2})); } # timer mins [secs]</pre>
<pre>timer() {
 local arg=${1/m/'*60+'}
 [[$arg = *+]] && arg+=0
 sleep $(($arg)
}</pre>

ToC: string-concat

Title: "+=" behaves differently from other shells

<p>In POSIX shell, "=" in code like <tt>var=content</tt> is a string
assignment, always. You can use <tt>var=$((content))</tt> for an
arithmetic assignment that mostly uses C language rules.</p>
<p>It stands to consider that the common shell extension "+=" as in
<tt>var+=content</tt> would always do string concatenation; it does
in mksh, but not in some other shells, in which, when <tt>var</tt> has
been declared integer, addition is done instead.</p>
<p>You can make the code portable by using "((…))" (a.k.a. <tt>let</tt>)
instead: <tt>((var += content))</tt> does arithmetic addition in
all shells involved.</p>

ToC: set-e

Title: I use "set -e" and my code unexpectedly errors out

<p>I personally recommend people to not use "<tt>set -e</tt>", as it
makes error handling more difficult. However, some insist. There have
been bugfixes (relative to e.g. oksh/loksh and posh) in this aspect,
and the user has to make sure <tt>$?</tt> is always 0 ASAP even after
a command that doesn't check it.</p>
<pre>istwo() {
    for i in "$@"; do
        test x"$i" = x"2" && echo two
    done
}
set -e
istwo 1

echo END</pre>

<p>This can be fixed by either adding an explicit "<tt>:</tt>" (or

"<tt>true</tt>") after the comparison, or even…</p>

<pre>test x"$i" = x"2" && echo two || :</pre>

<p>… or right after the <tt>done</tt> inside the function, but…</p>

<pre>test x"$i" != x"2" || echo two</pre>

<p>… negating the condition and using "<tt>||</tt>" is preferable.</p>

<p>Remember that Korn shell-style functions (with <tt>function</tt>

keyword and without parenthess) in AT&T ksh93

and mksh R51 and up have their own shell option scope, but while…</p>

<pre>function istwo {

    set +e

    …

}</pre>

<p>… might help in error handling, the return status of a function is

still the last errorlevel inside, so an explicit true ("<tt>:</tt>")

or, more explicitly, "<tt>return 0</tt>" at its end is still needed

if the caller runs under <tt>set -e</tt>.</p>

ToC: set-eo-pipefail

Title: I use "set -eo pipefail" and my code unexpectedly errors out

<p class="boxhead">Related to the above FAQ entry, using

<tt>set -o pipefail</tt> makes the following construct error out:</p>

<div class="boxtext">

<pre>

 set -e

 for x in 1 2; do

  false && echo $x

 done | cat

</pre>

</div><p class="boxfoot">This is because, while the <tt>&&</tt>

ensures that the inner command's failure is not taken, it sets the entire

<tt>for</tt><tt>done</tt> loop's errorlevel, which is passed on by

<tt>-o pipefail</tt>.</p>

<p>Invert the inner command:

<tt>true || echo $x</tt></p>

ToC: faq

Title: My question is not answered here!

Do read the mksh(1) manual page. You might also wish to read the <a

href="@@RELPATH@@ksh-chan.htm">homepage of the <tt>#ksh</tt> IRC channel

on Freenode which lists several resources for Korn or POSIX-compatible

shells in general. Or, contact us (developer and

users), for example via IRC.

ToC: contact
Title: How do I contact you (to say thanks)?

You can say hi in the <tt>#!/bin/mksh</tt> channel on Freenode <a
href="@@RELPATH@@irc.htm">IRC, although a <a
href="@@RELPATH@@danke.htm">donation wouldn't be amiss The <a
href="http://www.mail-archive.com/miros-mksh@mirbsd.org/">mailing
list can also be used.

Found in path(s):
* /opt/cola/permits/1063261178_1603927739.98/0/mksh-r59-tgz/mksh/mksh.faq
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*/

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No license file was found, but licenses were detected in source scan.

.\" $MirOS: src/bin/mksh/mksh.1,v 1.489 2020/04/14 22:45:21 tg Exp $
.\" $OpenBSD: ksh.1,v 1.160 2015/07/04 13:27:04 feinerer Exp $
.\"-
.\" Copyright © 2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009,
.\" 2010, 2011, 2012, 2013, 2014, 2015, 2016, 2017,
.\" 2018, 2019, 2020
.\" mirabilos <m@mirbsd.org>
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.\" direct, other damage, loss, or other issues arising in any way out
.\" of dealing in the work, even if advised of the possibility of such
.\" damage or existence of a defect, except proven that it results out

.\" of said person's immediate fault when using the work as intended.
.\"-
.\" Try to make GNU groff and AT&T nroff more compatible
.\" * ` generates ' in gnroff, so use \`
.\" * ' generates ' in gnroff, \' generates ´, so use *(aq
.\" * - generates in gnroff, \- generates , so .tr it to -
.\"   thus use - for hyphens and \- for minus signs and option dashes
.\" * ~ is size-reduced and placed atop in groff, so use *(TI
.\" * ^ is size-reduced and placed atop in groff, so use *(ha
.\" * \(en does not work in nroff, so use *(en for a solo en dash
.\" *   and *(EM for a correctly spaced em dash
.\" * <>| are problematic, so redefine and use *(Lt*(Gt*(Ba
.\" Also make sure to use \& *before* a punctuation char that is to not
.\" be interpreted as punctuation, and especially with two-letter words
.\" but also (after) a period that does not end a sentence ("e.g.\&").
.\" The section after the "doc" macropackage has been loaded contains
.\" additional code to convene between the UCB mdoc macropackage (and
.\" its variant as BSD mdoc in groff) and the GNU mdoc macropackage.
.\"
.\"
.\" Implement .Dd with the Mdocdate RCS keyword
.\"
.\"
.\" .Dd must come before definition of .Mx, because when called
.\" with -mandoc, it might implement .Mx itself, but we want to
.\" use our own definition. And .Dd must come *first*, always.
.\"
.\"
.\" Check which macro package we use, and do other -mdoc setup.
.\"
.\"
.\" Implement .Mx (MirBSD)
.\"
.\"-
.\" long integer ,
.\"
.\" This boils down to: feel free to use mksh.ico as application icon
.\" or shortcut for mksh or mksh/Win32 or OS/2; distro patches are ok
.\" (but we request they amend $KSH_VERSION when modifying mksh).
.\" Authors are Marshall Kirk McKusick (UCB), Rick Collette (ekkoBSD),
.\" mirabilos, Benny Siegert (MirBSD), Michael Langguth (mksh/Win32),
.\" KO Myung-Hun (mksh for OS/2).
.\"
.\" As far as MirBSD is concerned, the files themselves are free
.\" to modification and distribution under BSD/MirOS Licence, the
.\" restriction on use stems only from trademark law's requirement
.\" to protect it or lose it, which McKusick almost did.
.\"

.\" with vendor patches from insert-your-name-here,

Found in path(s):
* /opt/cola/permits/1063261178_1603927739.98/0/mksh-r59-tgz/mksh/mksh.1

1.3 speex 1.6.37

1.3.1 Available under license :

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 * stdio.c
 * by Mark Gates <mgates@nlanr.net>
 * and Ajay Tirumalla <tirumala@ncsa.uiuc.edu>
 * -------------------------------------------------------------------
 * input and output numbers, converting with kilo, mega, giga
 * ------------------------------------------------------------------ */
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1.6 edk-2 edk2-stable202111

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=== Start of sample patch email message ===


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Subject: [Repository/Branch PATCH] Module: Brief-single-line-summary


Full-commit-message


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---


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=== End of sample patch email message ===


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* git format-patch is one way to create this format


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   ===
   = Change Description / Commit Message / Patch Email =
   ===

   Your change description should use the standard format for a

commit message, and must include your "Signed-off-by" signature
and the "Contributed-under" message.

== Sample Change Description / Commit Message =

=== Start of sample patch email message ===

From: Contributor Name <contributor@example.com>
Subject: [PATCH] CodeModule: Brief-single-line-summary

Full-commit-message

Contributed-under: TianoCore Contribution Agreement 1.0
Signed-off-by: Contributor Name <contributor@example.com>

An extra message for the patch email which will not be considered part
of the commit message can be added here.

Patch content inline or attached

=== End of sample patch email message ===

=== Notes for sample patch email ===

* The first line of commit message is taken from the email's subject
  line following [PATCH]. The remaining portion of the commit message
  is the email's content until the '---' line.
* git format-patch is one way to create this format

=== Definitions for sample patch email ===

* "CodeModule" is a short idenfier for the affected code. For
  example MdePkg, or MdeModulePkg UsbBusDxe.
* "Brief-single-line-summary" is a short summary of the change.
* The entire first line should be less than ~70 characters.
* "Full-commit-message" a verbose multiple line comment describing
  the change. Each line should be less than ~70 characters.
* "Contributed-under" explicitely states that the contribution is
  made under the terms of the contribtion agreement. This
  agreement is included below in this document.
* "Signed-off-by" is the contributor's signature identifying them
  by their real/legal name and their email address.

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===

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# CoordinatorLayout resolves the behaviors of its child components with reflection.
-keep public class * extends android.support.design.widget.CoordinatorLayout$Behavior {
  public <init>(android.content.Context, android.util.AttributeSet);
  public <init>();
}

Make sure we keep annotations for CoordinatorLayout's DefaultBehavior
-keepattributes *Annotation*

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* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/proguard-rules.pro
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* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/tests/res/layout/design_fab.xml
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* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/res/drawable-anydpi-v21/design_ic_visibility_off.xml

* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/res/values-v21/styles.xml

* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/res/drawable-v21/design_password_eye.xml

* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/res/drawable/design_bottom_navigation_item_background.xml

* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/res/drawable/design_password_eye.xml

* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/res/drawable-v21/design_bottom_navigation_item_background.xml

* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/res/drawable/navigation_empty_icon.xml

* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/res/layout/design_bottom_navigation_item.xml

* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/res/drawable-anydpi-v21/design_ic_visibility.xml

* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/res/values/password_visibility.xml

* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/res/layout/design_text_input_password_icon.xml

* /opt/cola/permits/1107948750_1636651253.27/0/design-tar-gz/design/tests/res/layout/custom_snackbar_include.xml

1.13 libtiff 4.3.0

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1.14 openssl 1.1.1g

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1.15 firebase-messaging 28.4.1

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1.16 libzip 3.0-11

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<signature of Ty Coon>, 1 April 1990
Ty Coon, President of Vice

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1.19 boost 1.69.0

1.19.1 Available under license :

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#include <boost/mpl/push_back.hpp>

```cpp
#include <boost/mpl/quote.hpp>
#include <boost/mpl/transform.hpp>
#include <boost/mpl/vector.hpp>


template <typename X>
struct f { using type = X; };

template <int i>
struct t { };

using vector = <%= mpl_vector((1..input_size).to_a.map { |n| "t<#{n}>" }) %>;

using result = boost::mpl::transform<vector, boost::mpl::quote1<f>>::type;


int main() { }
```
```html
<!DOCTYPE html PUBLIC "-//W3C//DTD XHTML 1.0 Transitional//EN"
 "http://www.w3.org/TR/xhtml1/DTD/xhtml1-transitional.dtd">


<html xmlns="http://www.w3.org/1999/xhtml">
 <head>
  <meta http-equiv="Content-Type" content="text/html; charset=utf-8" />

  <title>License &#8212; Boost.HigherOrderFunctions 0.6 documentation</title>

  <link rel="stylesheet" href="../../_static/boostbook.css" type="text/css" />
  <link rel="stylesheet" href="../../_static/pygments.css" type="text/css" />

  <script type="text/javascript">
   var DOCUMENTATION_OPTIONS = {
    URL_ROOT:    '../../',
    VERSION:     '0.6',
    COLLAPSE_INDEX: false,
    FILE_SUFFIX: '.html',
    HAS_SOURCE:  true,
    SOURCELINK_SUFFIX: '.txt'
   };
  </script>
  <script type="text/javascript" src="../../_static/jquery.js"></script>
  <script type="text/javascript" src="../../_static/underscore.js"></script>
  <script type="text/javascript" src="../../_static/doctools.js"></script>
  <link rel="index" title="Index" href="../../genindex.html" />
  <link rel="search" title="Search" href="../../search.html" />
  <link rel="prev" title="Acknowledgements" href="acknowledgements.html" />
 </head>
 <body role="document">
```

```
<table cellpadding="2" width="100%"><tr>
<td valign="top"><img alt="Boost C++ Libraries" width="277" height="86"src="../../_static/boost.png"></td>
</tr></table>

<div class="spirit-nav">
<a accesskey="p"  href="acknowledgements.html"><img src="../../_static/prev.png" alt="Prev"></a>
<a accesskey="u" href="../index.html"><img src="../../_static/up.png" alt="Up"></a>
<a accesskey="h" href="../index.html"><img src="../../_static/home.png" alt="Home"></a>
<a accesskey="n"  ><img src="../../_static/next.png" alt="Next"></a>
</div>


  <div class="document">
 <div class="chapter">
   <div class="body" role="main">


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</div>


   </div>
 </div>
   <div class="clearer"></div>
  </div>
```

```
<div class="footer" role="contentinfo">
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<td align="left"></td>
<td align="right"><div class="copyright-footer">
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    </p>
</div></td>
</tr></table>
</div>
</body>
</html>
<!DOCTYPE html>
<html>
<head></head>
<body>
  <h3>
    Copyright Test
  </h3>
  <p class="copyright">
    1963, 1964, 1965 Jane Doe
  </p>
  <p class="copyright">
    2018 Joe Blow, John Coe
  </p>
  <p class="copyright">
    1977, 1985 Someone else
  </p>
</body>
</html>
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//

```
// See http://www.boost.org/libs/intrusive for documentation.
//
/////////////////////////////////////////////////////////////////////////////

#ifndef BOOST_INTRUSIVE_DETAIL_MPL_HPP
#define BOOST_INTRUSIVE_DETAIL_MPL_HPP

#ifndef BOOST_CONFIG_HPP
#  include <boost/config.hpp>
#endif

#if defined(BOOST_HAS_PRAGMA_ONCE)
#  pragma once
#endif

#include <boost/intrusive/detail/config_begin.hpp>
#include <boost/move/detail/type_traits.hpp>
#include <cstddef>

namespace boost {
namespace intrusive {
namespace detail {

using boost::move_detail::is_same;
using boost::move_detail::add_const;
using boost::move_detail::remove_const;
using boost::move_detail::remove_cv;
using boost::move_detail::remove_reference;
using boost::move_detail::add_reference;
using boost::move_detail::remove_pointer;
using boost::move_detail::add_pointer;
using boost::move_detail::true_type;
using boost::move_detail::false_type;
using boost::move_detail::enable_if_c;
using boost::move_detail::enable_if;
using boost::move_detail::disable_if_c;
using boost::move_detail::disable_if;
using boost::move_detail::is_convertible;
using boost::move_detail::if_c;
using boost::move_detail::if_;
using boost::move_detail::is_const;
using boost::move_detail::identity;
using boost::move_detail::alignment_of;
using boost::move_detail::is_empty;
using boost::move_detail::addressof;
using boost::move_detail::integral_constant;
using boost::move_detail::enable_if_convertible;
using boost::move_detail::disable_if_convertible;
```

```cpp
using boost::move_detail::bool_;
using boost::move_detail::true_;
using boost::move_detail::false_;
using boost::move_detail::yes_type;
using boost::move_detail::no_type;
using boost::move_detail::apply;
using boost::move_detail::eval_if_c;
using boost::move_detail::eval_if;
using boost::move_detail::unvoid_ref;
using boost::move_detail::add_const_if_c;

template<std::size_t S>
struct ls_zeros
{
  static const std::size_t value = (S & std::size_t(1)) ? 0 : (1 + ls_zeros<(S>>1u)>::value);
};

template<>
struct ls_zeros<0>
{
  static const std::size_t value = 0;
};

template<>
struct ls_zeros<1>
{
  static const std::size_t value = 0;
};

// Infrastructure for providing a default type for T::TNAME if absent.
#define BOOST_INTRUSIVE_INSTANTIATE_DEFAULT_TYPE_TMPLT(TNAME)     \
  template <typename T>                                 \
  struct boost_intrusive_has_type_ ## TNAME                \
  {                                                 \
    template <typename X>                             \
    static char test(int, typename X::TNAME*);              \
                                                    \
    template <typename X>                             \
    static int test(...);                              \
                                                    \
    static const bool value = (1 == sizeof(test<T>(0, 0)));     \
  };                                                \
                                                    \
  template <typename T, typename DefaultType>                \
  struct boost_intrusive_default_type_ ## TNAME              \
  {                                                 \
    struct DefaultWrap { typedef DefaultType TNAME; };         \
                                                    \
```

```
      typedef typename                                    \
        ::boost::intrusive::detail::if_c                  \
          < boost_intrusive_has_type_ ## TNAME<T>::value    \
          , T, DefaultWrap>::type::TNAME type;              \
   };                                                   \
   //

#define BOOST_INTRUSIVE_OBTAIN_TYPE_WITH_DEFAULT(INSTANTIATION_NS_PREFIX, T, \
TNAME, TIMPL)   \
    typename INSTANTIATION_NS_PREFIX                                      \
      boost_intrusive_default_type_ ## TNAME< T, TIMPL >::type              \
//

#define BOOST_INTRUSIVE_HAS_TYPE(INSTANTIATION_NS_PREFIX, T, TNAME)  \
    INSTANTIATION_NS_PREFIX                              \
      boost_intrusive_has_type_ ## TNAME< T >::value        \
//

#define BOOST_INTRUSIVE_INSTANTIATE_EVAL_DEFAULT_TYPE_TMPLT(TNAME)\
  template <typename T, typename DefaultType>               \
  struct boost_intrusive_eval_default_type_ ## TNAME          \
  {                                                  \
    template <typename X>                             \
    static char test(int, typename X::TNAME*);            \
                                                     \
    template <typename X>                             \
    static int test(...);                              \
                                                     \
    struct DefaultWrap                                \
    { typedef typename DefaultType::type TNAME; };           \
                                                     \
    static const bool value = (1 == sizeof(test<T>(0, 0)));    \
                                                     \
    typedef typename                                  \
      ::boost::intrusive::detail::eval_if_c              \
        < value                              \
        , ::boost::intrusive::detail::identity<T>         \
        , ::boost::intrusive::detail::identity<DefaultWrap>  \
        >::type::TNAME type;                         \
   };                                                 \
//

#define BOOST_INTRUSIVE_OBTAIN_TYPE_WITH_EVAL_DEFAULT(INSTANTIATION_NS_PREFIX, T,
TNAME, TIMPL) \
    typename INSTANTIATION_NS_PREFIX                                       \
      boost_intrusive_eval_default_type_ ## TNAME< T, TIMPL >::type               \
//
```

```
#define BOOST_INTRUSIVE_INTERNAL_STATIC_BOOL_IS_TRUE(TRAITS_PREFIX,
TYPEDEF_TO_FIND) \
template <class T>\
struct TRAITS_PREFIX##_bool\
{\
  template<bool Add>\
  struct two_or_three {yes_type _[2 + Add];};\
  template <class U> static yes_type test(...);\
  template <class U> static two_or_three<U::TYPEDEF_TO_FIND> test (int);\
  static const std::size_t value = sizeof(test<T>(0));\
};\
\
template <class T>\
struct TRAITS_PREFIX##_bool_is_true\
{\
  static const bool value = TRAITS_PREFIX##_bool<T>::value > sizeof(yes_type)*2;\
};\
//

#define BOOST_INTRUSIVE_HAS_STATIC_MEMBER_FUNC_SIGNATURE(TRAITS_NAME,
FUNC_NAME) \
  template <typename U, typename Signature> \
  class TRAITS_NAME \
  { \
  private: \
  template<Signature> struct helper;\
  template<typename T> \
  static ::boost::intrusive::detail::yes_type test(helper<&T::FUNC_NAME>*); \
  template<typename T> static ::boost::intrusive::detail::no_type test(...); \
  public: \
  static const bool value = sizeof(test<U>(0)) == sizeof(::boost::intrusive::detail::yes_type); \
  }; \
//

#define BOOST_INTRUSIVE_HAS_MEMBER_FUNC_CALLED(TRAITS_NAME, FUNC_NAME) \
template <typename Type> \
struct TRAITS_NAME \
{ \
  struct BaseMixin \
  { \
    void FUNC_NAME(); \
  }; \
  struct Base : public Type, public BaseMixin { Base(); }; \
  template <typename T, T t> class Helper{}; \
  template <typename U> \
  static ::boost::intrusive::detail::no_type  test(U*, Helper<void (BaseMixin::*)(), &U::FUNC_NAME>* = 0); \
  static ::boost::intrusive::detail::yes_type test(...); \
  static const bool value = sizeof(::boost::intrusive::detail::yes_type) == sizeof(test((Base*)(0))); \
```

};\
//

#define BOOST_INTRUSIVE_HAS_MEMBER_FUNC_CALLED_IGNORE_SIGNATURE(TRAITS_NAME, FUNC_NAME) \
BOOST_INTRUSIVE_HAS_MEMBER_FUNC_CALLED(TRAITS_NAME##_ignore_signature, FUNC_NAME) \
\
\
template <typename Type, class> \
struct TRAITS_NAME \
  : public TRAITS_NAME##_ignore_signature<Type> \
{};\
//

} //namespace detail
} //namespace intrusive
} //namespace boost

#include <boost/intrusive/detail/config_end.hpp>

#endif //BOOST_INTRUSIVE_DETAIL_MPL_HPP
==
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]

[section:mpl MPL Interoperability]

All the value based traits in this library conform to MPL's requirements
for an [@../../../../libs/mpl/doc/refmanual/integral-constant.html Integral Constant type].

Please note that these types no longer inherit from `mpl::true_` or `mpl::false_` etc, and the library
will no longer implicitly include any MPL header. However there is an implicit conversion from
`integral_constant` to the corresponding MPL types, therefore tag-dispatching that uses MPL types
in function overloads will still work as before.

[endsect]
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<link rel="up" href="../index.html" title="Chapter 1. Boost.TypeTraits">
<link rel="prev" href="intrinsics.html" title="Support for Compiler Intrinsics">
<link rel="next" href="examples.html" title="Examples">
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<p>
    All the value based traits in this library conform to MPL's requirements for
    an <a href="../../../../libs/mpl/doc/refmanual/integral-constant.html" target="_top">Integral
    Constant type</a>.
  </p>
<p>
    Please note that these types no longer inherit from <code class="computeroutput"><span
class="identifier">mpl</span><span class="special">::</span><span class="identifier">true_</span></code> or
    <code class="computeroutput"><span class="identifier">mpl</span><span class="special">::</span><span
class="identifier">false_</span></code> etc, and the library will no longer
    implicitly include any MPL header. However there is an implicit conversion
    from <code class="computeroutput"><span class="identifier">integral_constant</span></code> to the
    corresponding MPL types, therefore tag-dispatching that uses MPL types in function
    overloads will still work as before.
  </p>
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```
var group__group_ext_mpl =
[
  [ "integral_c", "structboost_1_1mpl_1_1integral__c.html", null ],
  [ "list", "structboost_1_1mpl_1_1list.html", null ],
  [ "vector", "structboost_1_1mpl_1_1vector.html", null ]
];
```

```
#include <boost/mpl/push_back.hpp>
#include <boost/mpl/vector.hpp>


template <int i>
struct t { };

using vector = <%= mpl_vector((1..input_size).to_a.map { |n| "t<#{n}>" }) %>;

int main() { }
```

```
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// http://www.boost.org/LICENSE_1_0.txt)
//
// See http://www.boost.org/libs/container for documentation.
//
/////////////////////////////////////////////////////////////////////////////

#ifndef BOOST_CONTAINER_CONTAINER_DETAIL_MPL_HPP
#define BOOST_CONTAINER_CONTAINER_DETAIL_MPL_HPP

#ifndef BOOST_CONFIG_HPP
#  include <boost/config.hpp>
#endif

#if defined(BOOST_HAS_PRAGMA_ONCE)
#  pragma once
#endif

#include <boost/container/detail/config_begin.hpp>
#include <boost/container/detail/workaround.hpp>
#include <boost/move/detail/type_traits.hpp>
#include <boost/intrusive/detail/mpl.hpp>
```

```cpp
#include <cstddef>

namespace boost {
namespace container {
namespace dtl {

using boost::move_detail::integral_constant;
using boost::move_detail::true_type;
using boost::move_detail::false_type;
using boost::move_detail::enable_if_c;
using boost::move_detail::enable_if;
using boost::move_detail::enable_if_convertible;
using boost::move_detail::disable_if_c;
using boost::move_detail::disable_if;
using boost::move_detail::disable_if_convertible;
using boost::move_detail::is_convertible;
using boost::move_detail::if_c;
using boost::move_detail::if_;
using boost::move_detail::identity;
using boost::move_detail::bool_;
using boost::move_detail::true_;
using boost::move_detail::false_;
using boost::move_detail::yes_type;
using boost::move_detail::no_type;
using boost::move_detail::bool_;
using boost::move_detail::true_;
using boost::move_detail::false_;
using boost::move_detail::unvoid_ref;
using boost::move_detail::and_;
using boost::move_detail::or_;
using boost::move_detail::not_;
using boost::move_detail::enable_if_and;
using boost::move_detail::disable_if_and;
using boost::move_detail::enable_if_or;
using boost::move_detail::disable_if_or;

template <class FirstType>
struct select1st
{
  typedef FirstType type;

  template<class T>
  const type& operator()(const T& x) const
  {  return x.first;   }

  template<class T>
  type& operator()(T& x)
```

```cpp
   {  return const_cast<type&>(x.first);   }
};

template <class T, class=void>
struct is_transparent
{
  static const bool value = false;
};

template <class T>
struct is_transparent<T, typename T::is_transparent>
{
  static const bool value = true;
};

template <typename C, typename K, typename R>
struct enable_if_transparent
  : boost::move_detail::enable_if_c<dtl::is_transparent<C>::value, R>
{};


} //namespace dtl {
} //namespace container {
} //namespace boost {

#include <boost/container/detail/config_end.hpp>

#endif   //#ifndef BOOST_CONTAINER_CONTAINER_DETAIL_MPL_HPP
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       VERSION:     '0.6',
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       FILE_SUFFIX: '.html',
       HAS_SOURCE:  true,
```

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      SOURCELINK_SUFFIX: '.txt'
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  <div class="document">
 <div class="chapter">
   <div class="body" role="main">


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   </div>
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      </p>
   </div></td>
    </tr></table>
   </div>
 </body>
</html>
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//
// See http://www.boost.org/libs/interprocess for documentation.
//
//////////////////////////////////////////////////////////////////////

#ifndef BOOST_INTERPROCESS_DETAIL_MPL_HPP
#define BOOST_INTERPROCESS_DETAIL_MPL_HPP

#ifndef BOOST_CONFIG_HPP
#  include <boost/config.hpp>
#endif
#
#if defined(BOOST_HAS_PRAGMA_ONCE)
#  pragma once
#endif

#include <cstddef>
```

```cpp
namespace boost {
namespace interprocess {
namespace ipcdetail {

template <class T, T val>
struct integral_constant
{
  static const T value = val;
  typedef integral_constant<T,val> type;
};

template< bool C_ >
struct bool_ : integral_constant<bool, C_>
{
  static const bool value = C_;
};

typedef bool_<true>       true_;
typedef bool_<false>      false_;

typedef true_  true_type;
typedef false_ false_type;

typedef char yes_type;
struct no_type
{
  char padding[8];
};

template <bool B, class T = void>
struct enable_if_c {
 typedef T type;
};

template <class T>
struct enable_if_c<false, T> {};

template <class Cond, class T = void>
struct enable_if : public enable_if_c<Cond::value, T> {};

template <class Cond, class T = void>
struct disable_if : public enable_if_c<!Cond::value, T> {};

template<
    bool C
  , typename T1
  , typename T2
  >
```

```cpp
struct if_c
{
   typedef T1 type;
};

template<
    typename T1
  , typename T2
  >
struct if_c<false,T1,T2>
{
   typedef T2 type;
};

template<
    typename T1
  , typename T2
  , typename T3
  >
struct if_
{
  typedef typename if_c<0 != T1::value, T2, T3>::type type;
};


template<std::size_t S>
struct ls_zeros
{
  static const std::size_t value = (S & std::size_t(1)) ? 0 : (1u + ls_zeros<(S >> 1u)>::value);
};

template<>
struct ls_zeros<0>
{
  static const std::size_t value = 0;
};

template<>
struct ls_zeros<1>
{
  static const std::size_t value = 0;
};

} //namespace ipcdetail {
} //namespace interprocess {
} //namespace boost {

#endif   //#ifndef BOOST_INTERPROCESS_DETAIL_MPL_HPP
```

```python
#!/usr/bin/env python
from subprocess import check_output as run
from datetime import datetime
from itertools import groupby
from operator import itemgetter
import re
import magic


def authors(filename):
    log = run(['git', 'log', '--follow',
            '--date=short','--format=%aN%x09%ad', filename],
            universal_newlines=True)
    for line in log.splitlines():
        author, date = line.split('\t')
        if author != 'fix-copyright.py':
            yield author, datetime.strptime(date, '%Y-%m-%d')


def new_copyright(filename, previous):
    def f():
        au = list(authors(filename))
        alldates = map(itemgetter(1), au)
        aup = sorted(au + map(lambda a: (a, None), previous), key=itemgetter(0))
        for author, records in groupby(aup, itemgetter(0)):
            dates = filter(None, map(itemgetter(1), records))
            if not dates: dates = alldates
            start = min(dates)
            end = max(dates)
            fmt = '{0}' if start.year == end.year else '{0}-{1}'
            line = 'Copyright ' + fmt.format(start.year, end.year) + ' ' + author
            key = (start, author)
            yield key, line
    return map(itemgetter(1), sorted(f()))


def fix_copyright(filename):
    # Find copyright block in original file
    prefix = set()
    names = []
    lines = []
    with open(filename, 'r') as f:
        content = list(f)
    for i, line in enumerate(content[:15]):
        m = re.match(r'^(?P<prefix>\W*)(\(c\))?\s*?copyright\s*(\(c\))?\s+\d{4}(\s*-\s*\d{4})?\s+(?P<name>.+?)\s*$',
line, re.IGNORECASE)
        if m:
            d = m.groupdict()
            prefix.add(d['prefix'])
            lines.append(i)
            names.append(d['name'].strip())
```

```
        if len(prefix) != 1:
            print 'Not found:', filename
            return
    prefix = list(prefix)[0]

    print filename
    new = iter(new_copyright(filename, names))
    with open(filename, 'w') as f:
        for i, line in enumerate(content):
            if i in lines:
                for repl in new:
                    print >>f, prefix + repl
            else:
                print >>f, line,
    pass


def all_files():
    ls = run(['git', 'ls-files'], universal_newlines=True)
    for filename in ls.splitlines():
        if magic.from_file(filename, mime=True).split('/')[0] == 'text':
            yield filename


for f in all_files():
    fix_copyright(f)
```
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[article Invalid copyright
[quickbook 1.5]
[copyright No year]

]

Maybe this should pass?

<!--

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-->

<!-- boost-no-inspect -->

<!-- HTML header for doxygen 1.8.9.1-->

<!DOCTYPE html PUBLIC "-//W3C//DTD XHTML 1.0 Transitional//EN"

"http://www.w3.org/TR/xhtml1/DTD/xhtml1-transitional.dtd">

<html xmlns="http://www.w3.org/1999/xhtml">

<head>

<meta http-equiv="Content-Type" content="text/xhtml;charset=UTF-8"/>

<meta http-equiv="X-UA-Compatible" content="IE=9"/>

<meta name="generator" content="Doxygen 1.8.11"/>

<title>Boost.Hana: Boost.MPL adapters</title>

<link href="tabs.css" rel="stylesheet" type="text/css"/>

<script type="text/javascript" src="jquery.js"></script>

<script type="text/javascript" src="dynsections.js"></script>

<link href="navtree.css" rel="stylesheet" type="text/css"/>

<script type="text/javascript" src="resize.js"></script>

<script type="text/javascript" src="navtreedata.js"></script>

<script type="text/javascript" src="navtree.js"></script>

<script type="text/javascript">

 $(document).ready(initResizable);

 $(window).load(resizeHeight);

</script>

<link href="search/search.css" rel="stylesheet" type="text/css"/>

<script type="text/javascript" src="search/searchdata.js"></script>

<script type="text/javascript" src="search/search.js"></script>

<script type="text/javascript">

 $(document).ready(function() { init_search(); });

</script>

<script type="text/x-mathjax-config">

 MathJax.Hub.Config({

  extensions: ["tex2jax.js"],

  jax: ["input/TeX","output/HTML-CSS"],

});

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MathJax.Hub.Config({

  "HTML-CSS": {

    linebreaks: {

       automatic: true,

       width: "75% container"

```
      }
    }
});
</script><script type="text/javascript" src="https://cdn.mathjax.org/mathjax/latest/MathJax.js"></script>
<link href="doxygen.css" rel="stylesheet" type="text/css" />
<!-- Additional javascript for drawing charts. -->
<script type="text/javascript" src="highcharts.js"></script>
<script type="text/javascript" src="highcharts-data.js"></script>
<script type="text/javascript" src="highcharts-exporting.js"></script>
<script type="text/javascript" src="chart.js"></script>
<script type="text/javascript" src="hana.js"></script>
</head>
<body>
<div id="top"><!-- do not remove this div, it is closed by doxygen! -->
<div id="titlearea">
<table cellspacing="0" cellpadding="0">
<tbody>
<tr style="height: 56px;">
 <td id="projectlogo"><img alt="Logo" src="Boost.png"/></td>
 <td style="padding-left: 0.5em;">
  <div id="projectname">Boost.Hana
   <span id="projectnumber">1.5.0</span>
  </div>
  <div id="projectbrief">Your standard library for metaprogramming</div>
 </td>
 <td>        <div id="MSearchBox" class="MSearchBoxInactive">
     <span class="left">
       <img id="MSearchSelect" src="search/mag_sel.png"
          onmouseover="return searchBox.OnSearchSelectShow()"
          onmouseout="return searchBox.OnSearchSelectHide()"
          alt=""/>
       <input type="text" id="MSearchField" value="Search" accesskey="S"
          onfocus="searchBox.OnSearchFieldFocus(true)"
          onblur="searchBox.OnSearchFieldFocus(false)"
          onkeyup="searchBox.OnSearchFieldChange(event)"/>
       </span><span class="right">
        <a id="MSearchClose" href="javascript:searchBox.CloseResultsWindow()"><img id="MSearchCloseImg"
border="0" src="search/close.png" alt=""/></a>
       </span>
     </div>
</td>
</tr>
</tbody>
</table>
</div>
<!-- end header part -->
<!-- Generated by Doxygen 1.8.11 -->
<script type="text/javascript">
```

```
var searchBox = new SearchBox("searchBox", "search",false,'Search');
</script>
</div><!-- top -->
<div id="side-nav" class="ui-resizable side-nav-resizable">
 <div id="nav-tree">
   <div id="nav-tree-contents">
     <div id="nav-sync" class="sync"></div>
   </div>
 </div>
 <div id="splitbar" style="-moz-user-select:none;"
     class="ui-resizable-handle">
 </div>
</div>
<script type="text/javascript">
$(document).ready(function(){initNavTree('group__group-ext-mpl.html','');});
</script>
<div id="doc-content">
<!-- window showing the filter options -->
<div id="MSearchSelectWindow"
   onmouseover="return searchBox.OnSearchSelectShow()"
   onmouseout="return searchBox.OnSearchSelectHide()"
   onkeydown="return searchBox.OnSearchSelectKey(event)">
</div>

<!-- iframe showing the search results (closed by default) -->
<div id="MSearchResultsWindow">
<iframe src="javascript:void(0)" frameborder="0"
     name="MSearchResults" id="MSearchResults">
</iframe>
</div>

<div class="header">
 <div class="summary">
<a href="#nested-classes">Classes</a>  </div>
 <div class="headertitle">
<div class="title">Boost.MPL adapters<div class="ingroups"><a class="el" href="group__group-
ext.html">External adapters</a></div></div>  </div>
</div><!--header-->
<div class="contents">
<a name="details" id="details"></a><h2 class="groupheader">Description</h2>
<p>Adapters for Boost.MPL containers. </p>
<table class="memberdecls">
<tr class="heading"><td colspan="2"><h2 class="groupheader"><a name="nested-classes"></a>
Classes</h2></td></tr>
<tr class="memitem:"><td class="memItemLeft" align="right" valign="top">struct  </td><td
class="memItemRight" valign="bottom"><a class="el"
href="structboost_1_1mpl_1_1integral__c.html">boost::mpl::integral_c< T, v ></a></td></tr>
<tr class="memdesc:"><td class="mdescLeft"> </td><td class="mdescRight">Adapter for IntegralConstants
```

from the Boost.MPL. More...
</td></tr>
<tr class="separator:"><td class="memSeparator" colspan="2">&#160;</td></tr>
<tr class="memitem:"><td class="memItemLeft" align="right" valign="top">struct &#160;</td><td
class="memItemRight" valign="bottom">boost::mpl::list< T
></td></tr>
<tr class="memdesc:"><td class="mdescLeft">&#160;</td><td class="mdescRight">Adapter for Boost.MPL lists.
More...
</td></tr>
<tr class="separator:"><td class="memSeparator" colspan="2">&#160;</td></tr>
<tr class="memitem:"><td class="memItemLeft" align="right" valign="top">struct &#160;</td><td
class="memItemRight" valign="bottom"><a class="el"
href="structboost_1_1mpl_1_1vector.html">boost::mpl::vector< T ></td></tr>
<tr class="memdesc:"><td class="mdescLeft">&#160;</td><td class="mdescRight">Adapter for Boost.MPL
vectors. More...
</td></tr>
<tr class="separator:"><td class="memSeparator" colspan="2">&#160;</td></tr>
</table>
</div><!-- contents -->
</div><!-- doc-content -->
<!--
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-->
<!-- boost-no-inspect -->
<!-- HTML footer for doxygen 1.8.9.1-->
<!-- start footer part -->
<div id="nav-path" class="navpath"><!-- id is needed for treeview function! -->

</div>
</body>
</html>
<?xml version="1.0" encoding="utf-8"?>

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-->

<section id="date_time.license">
 <title>Boost Date-Time Library License</title>
 <bridgehead renderas="sect2">Boost Date-Time Library License</bridgehead>
 <!--
 <ulink url="../../../index.htm">
  <imagedata align="left"
        format="GIF"
     fileref="../../../boost.png"
     alt="C++ Boost" />
   </ulink>-->

```
<!--hr /-->
<para>
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  library.
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</para>
<!--hr / -->
<ulink url="mailto:jeff@crystalclearsoftware.com">Jeff Garland</ulink>
&#169; 2000-2002
</section>
```

This is an attempt to acknowledge early contributions to the garbage
collector. Later contributions should instead be mentioned in
README.changes.

HISTORY -

 Early versions of this collector were developed as a part of research
projects supported in part by the National Science Foundation
and the Defense Advance Research Projects Agency.

The garbage collector originated as part of the run-time system for
the Russell programming language implementation. The first version of the
garbage collector was written primarily by Al Demers. It was then refined
and mostly rewritten, primarily by Hans-J. Boehm, at Cornell U.,
the University of Washington, Rice University (where it was first used for
C and assembly code), Xerox PARC, SGI, and HP Labs. However, significant
contributions have also been made by many others.

Some other contributors:

More recent contributors are mentioned in the modification history in
README.changes. My apologies for any omissions.

The SPARC specific code was originally contributed by Mark Weiser.
The Encore Multimax modifications were supplied by

Kevin Kenny (kenny@m.cs.uiuc.edu). The adaptation to the IBM PC/RT is largely
due to Vernon Lee, on machines made available to Rice by IBM.
Much of the HP specific code and a number of good suggestions for improving the
generic code are due to Walter Underwood.
Robert Brazile (brazile@diamond.bbn.com) originally supplied the ULTRIX code.
Al Dosser (dosser@src.dec.com) and Regis Cridlig (Regis.Cridlig@cl.cam.ac.uk)
subsequently provided updates and information on variation between ULTRIX
systems. Parag Patel (parag@netcom.com) supplied the A/UX code.
Jesper Peterson(jep@mtiame.mtia.oz.au), Michel Schinz, and
Martin Tauchmann (martintauchmann@bigfoot.com) supplied the Amiga port.
Thomas Funke (thf@zelator.in-berlin.de(?)) and
Brian D.Carlstrom (bdc@clark.lcs.mit.edu) supplied the NeXT ports.
Douglas Steel (doug@wg.icl.co.uk) provided ICL DRS6000 code.
Bill Janssen (janssen@parc.xerox.com) supplied the SunOS dynamic loader
specific code. Manuel Serrano (serrano@cornas.inria.fr) supplied linux and
Sony News specific code. Al Dosser provided Alpha/OSF/1 code. He and
Dave Detlefs(detlefs@src.dec.com) also provided several generic bug fixes.
Alistair G. Crooks(agc@uts.amdahl.com) supplied the NetBSD and 386BSD ports.
Jeffrey Hsu (hsu@soda.berkeley.edu) provided the FreeBSD port.
Brent Benson (brent@jade.ssd.csd.harris.com) ported the collector to
a Motorola 88K processor running CX/UX (Harris NightHawk).
Ari Huttunen (Ari.Huttunen@hut.fi) generalized the OS/2 port to
nonIBM development environments (a nontrivial task).
Patrick Beard (beard@cs.ucdavis.edu) provided the initial MacOS port.
David Chase, then at Olivetti Research, suggested several improvements.
Scott Schwartz (schwartz@groucho.cse.psu.edu) supplied some of the
code to save and print call stacks for leak detection on a SPARC.
Jesse Hull and John Ellis supplied the C++ interface code.
Zhong Shao performed much of the experimentation that led to the
current typed allocation facility. (His dynamic type inference code hasn't
made it into the released version of the collector, yet.)
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Beman Dawes (bdawes@acm.org)
Brad King (brad.king -at- kitware.com) (See Boost list message of Wed, 21 Jul 2004 11:15:46 -0400)
Brian Osman (osman -at- vvisions.com) (See CVS log)
Bruce Barr (schmoost -at- yahoo.com) (See Boost list of Mon, 16 Aug 2004 15:06:43 -0500)
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Cromwell D Enage (sponage -at- yahoo.com) (See Boost list message of August 12, 2004 11:49:13 AM EST)
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Daniel Nuffer (dan -at- nuffer.name)
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Gottfried Ganauge (Gottfried.Ganssauge -at- HAUFE.DE) (Alternative spelling of Gottfried Ganssauge)

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Gregory Colvin (gregory.colvin -at- oracle.com) (See Boost list message of Sat, 14 Aug 2004 10:57:00 +0100)

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Juergen Hunold (hunold -at- ive.uni-hannover.de) (See Boost List Message of Fri, 13 Aug 2004 19:39:55 +0200)

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Stefan Seefeld (seefeld -at- sympatico.ca)

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--- end ---
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-->

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=======

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```xml
<?xml version="1.0" encoding="UTF-8"?>
<!DOCTYPE article PUBLIC "-//Boost//DTD BoostBook XML V1.0//EN"
"http://www.boost.org/tools/boostbook/dtd/boostbook.dtd">
<article id="copyright_test" last-revision="DEBUG MODE Date: 2000/12/20 12:00:00 $"
xmlns:xi="http://www.w3.org/2001/XInclude">
 <title>Copyright Test</title>
 <articleinfo>
  <copyright>
   <year>1963</year> <year>1964</year> <year>1965</year> <holder>Jane Doe</holder>
  </copyright>
  <copyright>
   <year>2018</year> <holder>Joe Blow, John Coe</holder>
  </copyright>
  <copyright>
   <year>1977</year> <year>1985</year> <holder>Someone else</holder>
  </copyright>
 </articleinfo>
</article>
```

http_parser.c is based on src/http/ngx_http_parse.c from NGINX copyright
Igor Sysoev.

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```
// Copyright Louis Dionne 2013-2017
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#include <boost/mpl/fold.hpp>
#include <boost/mpl/push_back.hpp>
#include <boost/mpl/quote.hpp>
#include <boost/mpl/vector.hpp>


template <typename State, typename X>
struct f { using type = X; };

struct state { };

template <int i>
struct t { };

using vector = <%= mpl_vector((1..input_size).to_a.map { |n| "t<#{n}>" }) %>;

using result = boost::mpl::fold<vector, state, boost::mpl::quote2<f>>::type;
```

```
int main() { }
```
////
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http://www.boost.org/LICENSE_1_0.txt
////

[#mpl]
MPL Support, <boost/mp11/mpl.hpp>
:toc:
:toc-title:
:idprefix:

The header `<boost/mp11/mpl.hpp>`, when included, defines the
necessary support infrastructure for `mp_list` and `std::tuple`
to be valid link:../../../../libs/mpl[MPL] sequences.

NOTE: `mpl.hpp` is not included by `<boost/mp11.hpp>`.
[/==
 Boost.Geometry (aka GGL, Generic Geometry Library)

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 http://www.boost.org/LICENSE_1_0.txt)
==-/]
/*
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*
*/

#include "licence_info.hpp"
#include "bcp_imp.hpp"
#include "fileview.hpp"
#include <fstream>
#include <iomanip>

```cpp
#include <cstring>
#include <stdexcept>
#include <boost/lexical_cast.hpp>
#include <boost/filesystem/operations.hpp>
#include <boost/throw_exception.hpp>


//
// split_path is a small helper for outputting a path name,
// complete with a link to that path:
//
struct split_path
{
   const fs::path& root;
   const fs::path& file;
   split_path(const fs::path& r, const fs::path& f)
      : root(r), file(f){ }
private:
   split_path& operator=(const split_path&);
};

std::ostream& operator << (std::ostream& os, const split_path& p)
{
   os << "<a href=\"" << (p.root / p.file).string() << "\">" << p.file.string() << "</a>";
   return os;
}

std::string make_link_target(const std::string& s)
{
   // convert an arbitrary string into something suitable
   // for an <a> name:
   std::string result;
   for(unsigned i = 0; i < s.size(); ++i)
   {
      result.append(1, static_cast<std::string::value_type>(std::isalnum(s[i]) ? s[i] : '_'));
   }
   return result;
}


void bcp_implementation::output_license_info()
{
   std::pair<const license_info*, int> licenses = get_licenses();

   std::map<int, license_data>::const_iterator i, j;
   i = m_license_data.begin();
   j = m_license_data.end();

   std::ofstream os(m_dest_path.string().c_str());
```

```cpp
if(!os)
{
  std::string msg("Error opening ");
  msg += m_dest_path.string();
  msg += " for output.";
  std::runtime_error e(msg);
  boost::throw_exception(e);
}
os <<
  "<!DOCTYPE HTML PUBLIC \"-//W3C//DTD HTML 4.0 Transitional//EN\">\n"
  "<html>\n"
  "<head>\n"
  "<title>Boost Licence Dependency Information";
if(m_module_list.size() == 1)
{
  os << " for " << *(m_module_list.begin());
}
os <<
  "</title>\n"
  "</head>\n"
  "<body>\n"
  "<H1>Boost Licence Dependency Information";
if(m_module_list.size() == 1)
{
  os << " for " << *(m_module_list.begin());
}
os <<
  "</H1>\n"
  "<H2>Contents</h2>\n"
  "<pre><a href=\"#input\">Input Information</a>\n";
if(!m_bsl_summary_mode)
  os << "<a href=\"#summary\">Licence Summary</a>\n";
os << "<a href=\"#details\">Licence Details</a>\n";

while(i != j)
{
  // title:
  os << "   <A href=\"#" << make_link_target(licenses.first[i->first].license_name)
    << "\">" << licenses.first[i->first].license_name << "</a>\n";
  ++i;
}

os << "<a href=\"#files\">Files with no recognised license</a>\n"
  "<a href=\"#authors\">Files with no recognised copyright holder</a>\n";
if(!m_bsl_summary_mode)
{
  os <<
  "Moving to the Boost Software License...\n"
```

```
      " <a href=\"#bsl-converted\">Files that can be automatically converted to the Boost Software License</a>\n"
      " <a href=\"#to-bsl\">Files that can be manually converted to the Boost Software License</a>\n"
      " <a href=\"#not-to-bsl\">Files that can <b>NOT</b> be moved to the Boost Software License</a>\n"
      " <a href=\"#need-bsl-authors\">Authors we need to move to the Boost Software License</a>\n"
      "<a href=\"#copyright\">Copyright Holder Information</a>\n";
   }
   os <<
      "<a href=\"#depend\">File Dependency Information</a>\n"
      "</pre>";

   //
   // input Information:
   //
   os << "<a name=\"input\"></a><h2>Input Information</h2>\n";
   if(m_scan_mode)
      os << "<P>The following files were scanned for boost dependencies:<BR>";
   else
      os << "<P>The following Boost modules were checked:<BR>";

   std::list<std::string>::const_iterator si = m_module_list.begin();
   std::list<std::string>::const_iterator sj = m_module_list.end();
   while(si != sj)
   {
      os << *si << "<BR>";
      ++si;
   }
   os << "</p><p>The Boost path was: <code>" << m_boost_path.string() << "</code></P>";
   //
   // extract the boost version number from the boost directory tree,
   // not from this app (which may have been built from a previous
   // version):
   //
   fileview version_file(m_boost_path / "boost/version.hpp");
   static const boost::regex version_regex(
      "^[[:blank:]]*#[[:blank:]]*define[[:blank:]]+BOOST_VERSION[[:blank:]]+(\\d+)");
   boost::cmatch what;
   if(boost::regex_search(version_file.begin(), version_file.end(), what, version_regex))
   {
      int version = boost::lexical_cast<int>(what.str(1));
      os << "<p>The Boost version is: " << version / 100000 << "." << version / 100 % 1000 << "." << version % 100
<< "</P>\n";
   }

   //
   // output each license:
   //
   i = m_license_data.begin();
   j = m_license_data.end();
```

```
if(!m_bsl_summary_mode)
{
  //
  // start with the summary:
  //
  os << "<a name=\"summary\"></a><h2>Licence Summary</h2>\n";
  while(i != j)
  {
    // title:
    os <<
      "<H3>" << licenses.first[i->first].license_name << "</H3>\n";
    // license text:
    os << "<BLOCKQUOTE>" << licenses.first[i->first].license_text << "</BLOCKQUOTE>";
    // Copyright holders:
    os << "<P>This license is used by " << i->second.authors.size()
      << " authors and " << i->second.files.size()
      << " files <a href=\"#" << make_link_target(licenses.first[i->first].license_name) << "\">(see details)</a>";
    os << "</P></BLOCKQUOTE>\n";
    ++i;
  }
}
//
// and now the details:
//
i = m_license_data.begin();
j = m_license_data.end();
int license_index = 0;
os << "<a name=\"details\"></a><h2>Licence Details</h2>\n";
while(i != j)
{
  // title:
  os <<
    "<H3><A name=\"" << make_link_target(licenses.first[i->first].license_name)
    << "\"></a>" << licenses.first[i->first].license_name << "</H3>\n";
  // license text:
  os << "<BLOCKQUOTE>" << licenses.first[i->first].license_text << "</BLOCKQUOTE>";
  if(!m_bsl_summary_mode || (license_index >= 3))
  {
    // Copyright holders:
    os << "<P>This license is used by the following " << i->second.authors.size() << " copyright
holders:</P>\n<BLOCKQUOTE><P>";
    std::set<std::string>::const_iterator x, y;
    x = i->second.authors.begin();
    y = i->second.authors.end();
    while(x != y)
    {
      os << *x << "<BR>\n";
      ++x;
```

```
      }
      os << "</P></BLOCKQUOTE>\n";
      // Files using this license:
      os << "<P>This license applies to the following " << i->second.files.size() << "
files:</P>\n<BLOCKQUOTE><P>";
      std::set<fs::path, path_less>::const_iterator m, n;
      m = i->second.files.begin();
      n = i->second.files.end();
      while(m != n)
      {
        os << split_path(m_boost_path, *m) << "<br>\n";
        ++m;
      }
      os << "</P></BLOCKQUOTE>\n";
    }
    else
    {
      os << "<P>This license is used by " << i->second.authors.size() << " authors (list omitted for brevity).</P>\n";
      os << "<P>This license applies to " << i->second.files.size() << " files (list omitted for brevity).</P>\n";
    }
    ++license_index;
    ++i;
  }
  //
  // Output list of files not found to be under license control:
  //
  os << "<h2><a name=\"files\"></a>Files With No Recognisable Licence</h2>\n"
    "<P>The following " << m_unknown_licenses.size() << " files had no recognisable license
information:</P><BLOCKQUOTE><P>\n";
  std::set<fs::path, path_less>::const_iterator i2, j2;
  i2 = m_unknown_licenses.begin();
  j2 = m_unknown_licenses.end();
  while(i2 != j2)
  {
    os << split_path(m_boost_path, *i2) << "<br>\n";
    ++i2;
  }
  os << "</p></BLOCKQUOTE>";
  //
  // Output list of files with no found copyright holder:
  //
  os << "<h2><a name=\"authors\"></a>Files With No Recognisable Copyright Holder</h2>\n"
    "<P>The following " << m_unknown_authors.size() << " files had no recognisable copyright
holder:</P>\n<BLOCKQUOTE><P>";
  i2 = m_unknown_authors.begin();
  j2 = m_unknown_authors.end();
  while(i2 != j2)
  {
```

```
        os << split_path(m_boost_path, *i2) << "<br>\n";
        ++i2;
      }
    os << "</p></BLOCKQUOTE>";
    if(!m_bsl_summary_mode)
    {
      //
      // Output list of files that have been moved over to the Boost
      // Software License, along with enough information for human
      // verification.
      //
      os << "<h2><a name=\"bsl-converted\"></a>Files that can be automatically converted to the Boost Software
License</h2>\n"
        << "<P>The following " << m_converted_to_bsl.size() << " files can be automatically converted to the Boost
Software License, but require manual verification before they can be committed to CVS:</P>\n";
      if (!m_converted_to_bsl.empty())
      {
        typedef std::map<fs::path, std::pair<std::string, std::string>, path_less>
          ::const_iterator conv_iterator;
        conv_iterator i = m_converted_to_bsl.begin(),
                  ie = m_converted_to_bsl.end();
        int file_num = 1;
        while (i != ie)
        {
          os << "<P>[" << file_num << "] File: <tt>" << split_path(m_boost_path, i->first)
            << "</tt><br>\n<table border=\"1\">\n  <tr>\n    <td><pre>"
            << i->second.first << "</pre></td>\n    <td><pre>"
            << i->second.second << "</pre></td>\n  </tr>\n</table>\n";
          ++i;
          ++file_num;
        }
      }
      //
      // Output list of files that could be moved over to the Boost Software License
      //
      os << "<h2><a name=\"to-bsl\"></a>Files that could be converted to the Boost Software License</h2>\n"
        "<P>The following " << m_can_migrate_to_bsl.size() << " files could be manually converted to the Boost
Software License, but have not yet been:</P>\n<BLOCKQUOTE><P>";
      i2 = m_can_migrate_to_bsl.begin();
      j2 = m_can_migrate_to_bsl.end();
      while(i2 != j2)
      {
        os << split_path(m_boost_path, *i2) << "<br>\n";
        ++i2;
      }
      os << "</p></BLOCKQUOTE>";
      //
      // Output list of files that can not be moved over to the Boost Software License
```

```cpp
      //
      os << "<h2><a name=\"not-to-bsl\"></a>Files that can NOT be converted to the Boost Software
License</h2>\n"
         "<P>The following " << m_cannot_migrate_to_bsl.size() << " files cannot be converted to the Boost Software
License because we need the permission of more authors:</P>\n<BLOCKQUOTE><P>";
      i2 = m_cannot_migrate_to_bsl.begin();
      j2 = m_cannot_migrate_to_bsl.end();
      while(i2 != j2)
      {
        os << split_path(m_boost_path, *i2) << "<br>\n";
        ++i2;
      }
      os << "</p></BLOCKQUOTE>";
      //
      // Output list of authors that we need permission for to move to the BSL
      //
      os << "<h2><a name=\"need-bsl-authors\"></a>Authors we need for the BSL</h2>\n"
         "<P>Permission of the following authors is needed before we can convert to the Boost Software License. The
list of authors that have given their permission is contained in <code>more/blanket-
permission.txt</code>.</P>\n<BLOCKQUOTE><P>";
      std::copy(m_authors_for_bsl_migration.begin(), m_authors_for_bsl_migration.end(),
            std::ostream_iterator<std::string>(os, "<br>\n"));
      os << "</p></BLOCKQUOTE>";
      //
      // output a table of copyright information:
      //
      os << "<H2><a name=\"copyright\"></a>Copyright Holder Information</H2><table border=\"1\">\n";
      std::map<std::string, std::set<fs::path, path_less> >::const_iterator ad, ead;
      ad = m_author_data.begin();
      ead = m_author_data.end();
      while(ad != ead)
      {
        os << "<tr><td>" << ad->first << "</td><td>";
        std::set<fs::path, path_less>::const_iterator fi, efi;
        fi = ad->second.begin();
        efi = ad->second.end();
        while(fi != efi)
        {
          os << split_path(m_boost_path, *fi) << " ";
          ++fi;
        }
        os << "</td></tr>\n";
        ++ad;
      }
      os << "</table>\n";
   }

   //
```

```cpp
// output file dependency information:
//
os << "<H2><a name=\"depend\"></a>File Dependency Information</H2><BLOCKQUOTE><pre>\n";
std::map<fs::path, fs::path, path_less>::const_iterator dep, last_dep;
std::set<fs::path, path_less>::const_iterator fi, efi;
fi = m_copy_paths.begin();
efi = m_copy_paths.end();
// if in summary mode, just figure out the "bad" files and print those only:
std::set<fs::path, path_less> bad_paths;
if(m_bsl_summary_mode)
{
  bad_paths.insert(m_unknown_licenses.begin(), m_unknown_licenses.end());
  bad_paths.insert(m_unknown_authors.begin(), m_unknown_authors.end());
  bad_paths.insert(m_can_migrate_to_bsl.begin(), m_can_migrate_to_bsl.end());
  bad_paths.insert(m_cannot_migrate_to_bsl.begin(), m_cannot_migrate_to_bsl.end());
  typedef std::map<fs::path, std::pair<std::string, std::string>, path_less>
    ::const_iterator conv_iterator;
  conv_iterator i = m_converted_to_bsl.begin(),
            ie = m_converted_to_bsl.end();
  while(i != ie)
  {
    bad_paths.insert(i->first);
    ++i;
  }
  fi = bad_paths.begin();
  efi = bad_paths.end();
  os << "<P>For brevity, only files not under the BSL are shown</P>\n";
}
while(fi != efi)
{
  os << split_path(m_boost_path, *fi);
  dep = m_dependencies.find(*fi);
  last_dep = m_dependencies.end();
  std::set<fs::path, path_less> seen_deps;
  if (dep != last_dep)
    while(true)
      {
        os << " -> ";
        if(fs::exists(m_boost_path / dep->second))
          os << split_path(m_boost_path, dep->second);
        else if(fs::exists(dep->second))
          os << split_path(fs::path(), dep->second);
        else
          os << dep->second.string();
        if(seen_deps.find(dep->second) != seen_deps.end())
          {
            os << " <I>(Circular dependency!)</I>";
            break; // circular dependency!!!
```

```
        }
      seen_deps.insert(dep->second);
      last_dep = dep;
      dep = m_dependencies.find(dep->second);
      if((dep == m_dependencies.end()) || (0 == compare_paths(dep->second, last_dep->second)))
        break;
      }
    os << "\n";
    ++fi;
  }
  os << "</pre></BLOCKQUOTE>\n";

  os << "</body></html>\n";

  if(!os)
  {
    std::string msg("Error writing to ");
    msg += m_dest_path.string();
    msg += ".";
    std::runtime_error e(msg);
    boost::throw_exception(e);
  }

}
```

1.20 leveldb 1.22

1.20.1 Available under license :

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1.21 zlib 1.2.8

1.21.1 Available under license :

/* zlib.h -- interface of the 'zlib' general purpose compression library
   version 1.2.11, January 15th, 2017

   Copyright (C) 1995-2017 Jean-loup Gailly and Mark Adler

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   Jean-loup Gailly   Mark Adler
   jloup@gzip.org   madler@alumni.caltech.edu

   The data format used by the zlib library is described by RFCs (Request for
   Comments) 1950 to 1952 in the files http://tools.ietf.org/html/rfc1950
   (zlib format), rfc1951 (deflate format) and rfc1952 (gzip format).
*/

1.22 android-support 28.0.0

1.22.1 Available under license :

No license file was found, but licenses were detected in source scan.

/*

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*

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*/

Found in path(s):
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Int2.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Long2.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Float2.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Int3.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Short4.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Long4.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Float4.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Long3.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Int4.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Short3.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Short2.java
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* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/MediaDescriptionCompatApi23.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/ThemedYellowActivity.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/ScriptIntrinsicHistogram.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/testutils/TestUtilsMatchers.java

* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/ScriptIntrinsicBLAS.java
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* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/rastermill/FrameSequence.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Type.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/RatingCompat.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/rastermill/FrameSequenceDrawable.java
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 */
/**
   * Sends a proprietary event to all MediaControllers listening to this
   * Session. It's up to the Controller/Session owner to determine the meaning
   * of any events.
   *
   * @param event The name of the event to send
   * @param extras Any extras included with the event
   */
```

Found in path(s):
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* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/v8/renderscript/Matrix3f.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
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* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/testlib/util/PollingCheck.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/client/MediaBrowserCompatTest.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/service/ServiceBroadcastReceiver.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/testlib/util/IntentUtil.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/client/ClientBroadcastReceiver.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/testlib/MediaSessionConstants.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/client/AudioAttributesCompatTest.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/service/MediaSessionCompatCallbackTest.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/service/StubMediaBrowserServiceCompat.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/testlib/VersionConstants.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/testlib/MediaControllerConstants.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/client/MediaItemTest.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/service/StubMediaBrowserServiceCompatWithDelayedMediaSession.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/client/PlaybackStateCompatTest.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/mediacompat/testlib/MediaBrowserConstants.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
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* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/MediaMetadataCompat.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/session/MediaSessionCompatApi23.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/session/PlaybackStateCompatApi21.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/MediaMetadataCompatApi21.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/MediaDescriptionCompatApi21.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/session/MediaSessionCompatApi21.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/session/PlaybackStateCompat.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/session/PlaybackStateCompatApi22.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/session/MediaSessionCompatApi22.java
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* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/ScriptIntrinsicBlur.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/BaseObj.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/ScriptGroup.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/ScriptIntrinsicColorMatrix.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Double3.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/ScriptIntrinsicLUT.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/ScriptIntrinsicBlend.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Sampler.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/ScriptIntrinsicYuvToRGB.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/ScriptIntrinsicConvolve5x5.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/ScriptIntrinsic3DLUT.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Byte2.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/FieldPacker.java
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* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Byte4.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Double4.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/Byte3.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v8/renderscript/ScriptC.java

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zip/support/v4/BaseTestActivity.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/v4/testutils/TextViewActions.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/v4/media/session/MediaSessionCompatApi24.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/v4/media/ParceledListSliceAdapterApi21.java
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zip/support/v8/renderscript/RSIllegalArgumentException.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-
zip/support/v8/renderscript/RSInvalidStateException.java
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* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/session/MediaControllerCompatApi21.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/MediaBrowserCompat.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/MediaBrowserCompatApi26.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/MediaBrowserCompatApi21.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/MediaBrowserCompatApi23.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/os/ResultReceiver.java
* /opt/ws_local/PERMITS_SQL/1076190557_1596614346.35/0/android-support-zip/support/v4/media/session/MediaControllerCompat.java
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1.26 optee-client 3.8.0

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1.27 zlib 0.0.0

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1.28 protobuf v3.6.1

1.29 appcompat 1.3.1

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/drawable/avd_heart_fill.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/androidTest/res/drawable/animated_state_list_with_avd.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/androidTest/res/values/colors.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/androidTest/res/drawable/animated_state_list_density.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/empty.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/androidTest/res/drawable/ic_heart_empty.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/androidTest/res/drawable/asl_heart_embedded.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/drawable/ic_heart_empty.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/view_attribute_layout.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/androidTest/res/drawable/vector_drawable_grouping_1.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/drawable/ic_heart_full.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/androidTest/res/drawable/animation_list_transition_1.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/androidTest/res/anim/animation_grouping_1_01.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/drawable/abc_switch_thumb_material.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/layout/abc_alert_dialog_button_bar_material.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/main/res/values/dimens_material.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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resources/src/main/java/androidx/appcompat/widget/ResourceManagerInternal.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-
resources/build.gradle
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-benchmark/src/androidTest/AndroidManifest.xml

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/color/color_state_theme_coloraccent.xml

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/layout/abc_list_menu_item_radio.xml

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/layout/abc_list_menu_item_checkbox.xml

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gz/appcompat/appcompat/src/main/res/color/abc_secondary_text_material_light.xml
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public/values/public_styles.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/values-zh-rTW/strings.xml

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/values-te/strings.xml

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/values-es/strings.xml

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/main/AndroidManifest.xml

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```

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/view/menu/MenuWrapperICS.java

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/view/ActionBarPolicy.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/view/menu/SubMenuWrapperICS.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/app/ActionBar.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/view/menu/MenuBuilder.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/view/menu/BaseMenuWrapper.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/ActionBarOverlayLayout.java

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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lint/src/test/kotlin/androidx/appcompat/lint/res/ImageButtonTintDetectorTest.kt
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-
lint/src/test/kotlin/androidx/appcompat/lint/view/OnClickXmlDetectorTest.kt
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-
lint/src/main/kotlin/androidx/appcompat/res/ColorStateListLoadingDetector.kt
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-lint/src/main/kotlin/androidx/appcompat/widget/TextViewCompoundDrawablesApiDetector.kt

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/drawable/red_square.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/anim/btn_radio_to_on_mtrl_ring_outer_animation.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/drawable/abc_ic_menu_overflow_material.xml

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gz/appcompat/appcompat/src/androidTest/res/layout/appcompat_icons_activity.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/DialogTitle.java

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```
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```

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/main/java/androidx/appcompat/content/res/AppCompatResources.java

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Found in path(s):
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/color/abc_btn_colored_borderless_text_material.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/appcompat_imageview_activity.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/drawable-v21/abc_dialog_material_background.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/drawable/test_vector_state.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/color/color_state_list_sand.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/drawable-v21/abc_edit_text_material.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/color/color_state_list_lilac.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/color-v23/color_state_list_themed_attrs.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/color-v23/abc_btn_colored_text_material.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/drawable/test_background_green.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/layout_imageview_vector.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/appcompat_button_activity.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/alert_dialog_custom_title.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/color/abc_btn_colored_text_material.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/popup_window_item.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/color-v23/abc_btn_colored_borderless_text_material.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/drawable/test_vector_left_white_right_black.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/appcompat_vectordrawable_integration.xml

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/layout_radiobutton_vector.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/layout_contextwrapperparent_imageview_vector.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/drawable/abc_dialog_material_background.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/drawable/test_vector_on.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/drawer_dynamic_content_double_start.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/color-
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gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/MenuPopupWindow.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-

gz/appcompat/appcompat/src/main/java/androidx/appcompat/app/ResourcesFlusher.java

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gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/widget/AppCompatAttributeTest.kt

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-

gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeCustomAttachBaseContextTest

Case.kt

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-

gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeRotateDoesNotRecreateActivity

TestCase.kt

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-

gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/EmptyOptionsPanelActivity.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-

gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModePreventOverrideConfigActivity.

java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeRotateDoesNotRecreateActivity.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-lint/build.gradle
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/WindowDecorBeforeOnCreateAppCompatActivity.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/androidTest/java/androidx/appcompat/content/res/AppCompatResourcesTestCase.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeCustomAttachBaseContextActivity.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/androidTest/java/androidx/appcompat/widget/TintResourcesTest.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/EmptyOptionsPanelTest.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeLateOnCreateActivity.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/testutils/NightModeUtils.kt
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeLateOnCreateTestCase.kt
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/test/java/androidx/appcompat/app/AppCompatResourcesRobolectricTest.kt
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/WindowDecorBeforeOnCreateTestCase.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModePreventOverrideConfigTestCase.kt
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-lint/src/main/kotlin/androidx/appcompat/res/ColorStateListAlphaDetector.kt
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeForegroundDialogTestCase.kt
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeRotateRecreatesActivityWithConfigTestCase.kt
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeUiModeConfigChangesTestCase.kt
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/androidTest/java/androidx/appcompat/graphics/drawable/AnimatedStateListDrawableCompatTest.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-lint/src/main/kotlin/androidx/appcompat/AppCompatIssueRegistry.kt
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeUiModeConfigChangesActivity.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-benchmark/src/androidTest/java/androidx/appcompat/benchmark/ViewInflationBenchmark.kt

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/ActivityUnitTestSetActivityContextTest.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeDefaultOnlyTestCase.kt

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/app/NightModeLocalOnlyTestCase.kt

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/drawable/abc_ic_search_api_material.xml

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aapt is not able to read app::actionViewClass and app:actionProviderClass to produce proguard
keep rules. Add a commonly used SearchView to the keep list until b/109831488 is resolved.
-keep class androidx.appcompat.widget.SearchView { <init>(...); }

Never inline methods, but allow shrinking and obfuscation.

-keepclassmembernames,allowobfuscation,allowshrinking class
androidx.appcompat.widget.AppCompatTextViewAutoSizeHelper$Impl* {
 <methods>;
}

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gz/appcompat/appcompat/src/main/res/layout/abc_search_dropdown_item_icons_2line.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/values/arrays.xml

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/appcompat_button_autosize_activity.xml

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/res/anim/abc_tooltip_exit.xml

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/appcompat_inflater_activity.xml

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/res/layout/textview_autosize_maxlines.xml

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gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/ScrollingTabContainerView.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/main/java/androidx/appcompat/view/menu/MenuPresenter.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/main/java/androidx/appcompat/view/CollapsibleActionView.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/AbsActionBarView.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/main/java/androidx/appcompat/view/menu/BaseMenuPresenter.java
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/main/java/androidx/appcompat/app/AppCompatDelegateImpl.java
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/ActivityChooserModel.java
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gz/appcompat/appcompat/src/main/res/drawable/abc_ic_ab_back_material.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-

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This is an optimized layout for a screen, with the minimum set of features
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/main/res/anim/abc_slide_in_bottom.xml

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/main/res/anim/abc_slide_in_top.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/app/ActionBarDrawerToggleHoneycomb.java

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/app/WindowDecorActionBar.java

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/ActionMenuView.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/text/AllCapsTransformationMethod.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/app/AppCompatDelegate.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/LinearLayoutCompat.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/graphics/drawable/DrawerArrowDrawable.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/TintTypedArray.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/view/StandaloneActionMode.java

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/PopupMenu.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/AppCompatButton.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/AppCompatSpinner.java

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/DecorContentParent.java

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/app/ToolbarActionBar.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-

resources/src/main/java/androidx/appcompat/widget/DrawableUtils.java

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/FitWindowsLinearLayout.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/widget/AppCompatAutoCompleteTextView.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/main/java/androidx/appcompat/app/ActionBarDrawerToggle.java

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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/integration-tests/receive-content-testapp/src/main/res/drawable/thumbnail_background.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/integration-tests/receive-content-testapp/src/main/res/layout/attachment.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/integration-tests/receive-content-testapp/src/main/res/values/colors.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/androidTest/res/color/color_state_lilac_alpha.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/main/res/layout/abc_action_bar_title_item.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/androidTest/res/layout/layout_android_theme_with_include.xml
* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-
gz/appcompat/appcompat/src/androidTest/res/layout/layout_android_theme_included_view.xml
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* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/widget/AppCompatEditTextActivity.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/main/java/androidx/appcompat/graphics/drawable/StateListDrawable.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/main/java/androidx/appcompat/graphics/drawable/DrawableContainer.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat-resources/src/main/java/androidx/appcompat/graphics/drawable/AnimatedStateListDrawableCompat.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/widget/AppCompatCheckBoxActivity.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/widget/ToolbarTest.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/widget/AppCompatCheckBoxTest.java

* /opt/cola/permits/1201534898_1636571666.82/0/appcompat-src-tar-gz/appcompat/appcompat/src/androidTest/java/androidx/appcompat/widget/ToolbarTestActivity.java

1.30 libphonenumber 8.10.7

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* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/SingleFileMetadataSourceImpl.java
* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/MetadataSource.java
* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/MultiFileMetadataSourceImpl.java
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* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/PhoneNumberMatcher.java
* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/PhoneNumberMatch.java
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jar/com/google/i18n/phonenumbers/MetadataManager.java
* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-
jar/com/google/i18n/phonenumbers/AlternateFormatsCountryCodeSet.java
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* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/internal/RegexBasedMatcher.java

* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/MetadataLoader.java

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* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/NumberParseException.java

* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/AsYouTypeFormatter.java

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* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/CountryCodeToRegionCodeMap.java

* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/Phonenumber.java

* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/Phonemetadata.java

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* /opt/ws_local/PERMITS_SQL/1021498965_1591373983.59/0/libphonenumber-8-10-7-sources-jar/com/google/i18n/phonenumbers/ShortNumbersRegionCodeSet.java

1.31 libexif 0.6.21

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1.32 zlib 1.6.37

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1.33 bzip2 1.0.6

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Julian Seward, Cambridge, UK.
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bzip2/libbzip2 version 1.0.2 of 30 December 2001

```
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  minibz2
    libbz2.dll test program.
    by Yoshioka Tsuneo (tsuneo@rr.iij4u.or.jp)
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  usage: minibz2 [-d] [-{1,2,..9}] [[srcfilename] destfilename]
*/
```

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1.34 libsepol 2.9

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1.35 hostapd 2.10-devel-10

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1.36 constraintlayout 2.1.0

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1.37 flutter 1.22.3

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1.39 blas 3.9.0-r1

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C++ Big Integer Library
(see ChangeLog for version)

http://mattmccutchen.net/bigint/

Written and maintained by Matt McCutchen <matt@mattmccutchen.net>

You can use this library in a C++ program to do arithmetic on integers of size
limited only by your computer's memory. The library provides BigUnsigned and
BigInteger classes that represent nonnegative integers and signed integers,
respectively. Most of the C++ arithmetic operators are overloaded for these
classes, so big-integer calculations are as easy as:

```
#include "BigIntegerLibrary.hh"

BigInteger a = 65536;
cout << (a * a * a * a * a * a * a * a);
```

(prints 340282366920938463463374607431768211456)

The code in `sample.cc' demonstrates the most important features of the library.
To get started quickly, read the code and explanations in that file and run it.
If you want more detail or a feature not shown in `sample.cc', consult the
consult the actual header and source files, which are thoroughly commented.

This library emphasizes ease of use and clarity of implementation over speed;
some users will prefer GMP (http://swox.com/gmp/), which is faster. The code is
intended to be reasonably portable across computers and modern C++ compilers; in
particular, it uses whatever word size the computer provides (32-bit, 64-bit, or
otherwise).

Compiling programs that use the library

The library consists of a folder full of C++ header files (`.hh') and source
files (`.cc').  Your own programs should `#include' the necessary header files
and link with the source files. A makefile that builds the sample program
(`sample.cc') is included; you can adapt it to replace the sample with your own
program.

Alternatively, you can use your own build system or IDE. In that case, you must
put the library header files where the compiler will find them and arrange to
have your program linked with the library source files; otherwise, you will get
errors about missing header files or "undefined references". To learn how to do
this, consult the documentation for the build system or IDE; don't bother asking
me. Adding all the library files to your project will work in many IDEs but may
not be the most desirable approach.

Resources

The library's Web site (above) provides links to released versions, the current
development version, and a mailing list for release announcements, questions,
bug reports, and other discussion of the library. I would be delighted to hear
from you if you like this library and/or find a good use for it.

Bugs and enhancements

The library has been tested by me and others but is by no means bug-free. If
you find a bug, please report it, whether it comes in the form of compiling
trouble, a mathematically inaccurate result, or a memory-management blooper
(since I use Java, these are altogether too common in my C++). I generally fix
all reported bugs. You are also welcome to request enhancements, but I am
unlikely to do substantial amounts of work on enhancements at this point.

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* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/WebTextView.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/CookieSyncManager.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/CallbackProxy.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/Plugin.java
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* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/WebView.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/BrowserFrame.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/URLUtil.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/CookieManager.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/WebIconDatabase.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/CacheManager.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/JWebCoreJavaBridge.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/WebHistoryItem.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/DateSorter.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/ByteArrayBuilder.java
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* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/WebViewFactoryProvider.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/WebViewProvider.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/WebSettingsClassic.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/WebViewClassic.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/AutoCompletePopup.java
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* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/PluginStub.java
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* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/GeolocationPermissions.java
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* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/KeyStoreHandler.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/ViewStateSerializer.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/SearchBoxImpl.java
* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-

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* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/ConsoleMessage.java

* /opt/cola/permits/1205110390_1636579488.54/0/base-a5408e6-core-java-android-webkit-tar-gz/ZoomControlEmbedded.java

1.52 websocketpp 0.8.1

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md5.hpp is a reformulation of the md5.h and md5.c code from
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* From: Wilco Dijkstra <Wilco.Dijkstra@ntlworld.com>
* Date: Fri, Jun 24, 2011 at 3:20 AM
* Subject: Re: sqrt routine
* To: Kevin Ma <kma@google.com>
* Hi Kevin,
* Thanks for asking. Those routines are public domain (originally posted to
* comp.sys.arm a long time ago), so you can use them freely for any purpose.
* Cheers,
* Wilco
*
* ----- Original Message -----
* From: "Kevin Ma" <kma@google.com>
* To: <Wilco.Dijkstra@ntlworld.com>
* Sent: Thursday, June 23, 2011 11:44 PM
* Subject: Fwd: sqrt routine
* Hi Wilco,
* I saw your sqrt routine from several web sites, including
* http://www.finesse.demon.co.uk/steven/sqrt.html.
* Just wonder if there's any copyright information with your Successive
* approximation routines, or if I can freely use it for any purpose.
* Thanks.
* Kevin
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//* Enhancements by Stanley Yamane:
//*   o reverse lookup table for the decode function
//*   o reserve string buffer space in advance
//*
//***

Files:
base/md5.cc

base/md5.h

License:
/*
* This code implements the MD5 message-digest algorithm.
* The algorithm is due to Ron Rivest. This code was
* written by Colin Plumb in 1993, no copyright is claimed.
* This code is in the public domain; do with it what you wish.
*

Files:
base/sha1.cc
base/sha1.h

License:
/*
* SHA-1 in C
* By Steve Reid <sreid@sea-to-sky.net>
* 100% Public Domain
*
* -----------------
* Modified 7/98
* By James H. Brown <jbrown@burgoyne.com>
* Still 100% Public Domain
*

Files:
base/sigslot.cc
base/sigslot.h

License:
// sigslot.h: Signal/Slot classes
//
// Written by Sarah Thompson (sarah@telergy.com) 2002.
//
// License: Public domain. You are free to use this code however you like, with
// the proviso that the author takes on no responsibility or liability for any
// use.

Files:
common_audio/signal_processing/spl_sqrt_floor.c
common_audio/signal_processing/spl_sqrt_floor_arm.S

License:
/*
* Written by Wilco Dijkstra, 1996. The following email exchange establishes the
* license.
*

* From: Wilco Dijkstra <Wilco.Dijkstra@ntlworld.com>

* Date: Fri, Jun 24, 2011 at 3:20 AM

* Subject: Re: sqrt routine

* To: Kevin Ma <kma@google.com>

* Hi Kevin,

* Thanks for asking. Those routines are public domain (originally posted to

* comp.sys.arm a long time ago), so you can use them freely for any purpose.

* Cheers,

* Wilco

*

* ----- Original Message -----

* From: "Kevin Ma" <kma@google.com>

* To: <Wilco.Dijkstra@ntlworld.com>

* Sent: Thursday, June 23, 2011 11:44 PM

* Subject: Fwd: sqrt routine

* Hi Wilco,

* I saw your sqrt routine from several web sites, including

* http://www.finesse.demon.co.uk/steven/sqrt.html.

* Just wonder if there's any copyright information with your Successive

* approximation routines, or if I can freely use it for any purpose.

* Thanks.

* Kevin

*/

Files:

modules/audio_coding/codecs/g711/main/source/g711.c

modules/audio_coding/codecs/g711/main/source/g711.h

License:

/*

* SpanDSP - a series of DSP components for telephony

*

* g711.h - In line A-law and u-law conversion routines

*

* Written by Steve Underwood <steveu@coppice.org>

*

* Copyright (C) 2001 Steve Underwood

*

* Despite my general liking of the GPL, I place this code in the

* public domain for the benefit of all mankind - even the slimy

* ones who might try to proprietize my work and use it to my

* detriment.

*/

Files:

modules/audio_coding/codecs/g722/main/source/g722_decode.c

modules/audio_coding/codecs/g722/main/source/g722_enc_dec.h

modules/audio_coding/codecs/g722/main/source/g722_encode.c

License:
/*
* SpanDSP - a series of DSP components for telephony
*
* g722_decode.c - The ITU G.722 codec, decode part.
*
* Written by Steve Underwood <steveu@coppice.org>
*
* Copyright (C) 2005 Steve Underwood
*
* Despite my general liking of the GPL, I place my own contributions
* to this code in the public domain for the benefit of all mankind -
* even the slimy ones who might try to proprietize my work and use it
* to my detriment.
*
* Based in part on a single channel G.722 codec which is:
*
* Copyright (c) CMU 1993
* Computer Science, Speech Group
* Chengxiang Lu and Alex Hauptmann
*/

Files:
modules/audio_coding/codecs/isac/main/source/fft.c

License:
/*
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*   Queen's Univ at Kingston (Canada)
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*

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* should make their way back to the general Internet community so
* that everyone benefits.
*/

Files:
modules/audio_device/mac/portaudio/pa_memorybarrier.h
modules/audio_device/mac/portaudio/pa_ringbuffer.c
modules/audio_device/mac/portaudio/pa_ringbuffer.h

License:
/*
* Id
* Portable Audio I/O Library
* Memory barrier utilities
*
* Author: Bjorn Roche, XO Audio, LLC
*
* This program uses the PortAudio Portable Audio Library.
* For more information see: http://www.portaudio.com
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* they can be incorporated into the canonical version. It is also
* requested that these non-binding requests be included along with the
* license above.
*/

/*
* Id
* Portable Audio I/O Library
* Ring Buffer utility.
*
* Author: Phil Burk, http://www.softsynth.com
* modified for SMP safety on Mac OS X by Bjorn Roche
* modified for SMP safety on Linux by Leland Lucius
* also, allowed for const where possible
* modified for multiple-byte-sized data elements by Sven Fischer
*
* Note that this is safe only for a single-thread reader and a
* single-thread writer.
*
* This program uses the PortAudio Portable Audio Library.
* For more information see: http://www.portaudio.com
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*/

Files:

common_audio/fft4g.c

modules/audio_processing/aec/aec_rdft.c

License:

/*

* http://www.kurims.kyoto-u.ac.jp/~ooura/fft.html

* Copyright Takuya OOURA, 1996-2001

*

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*/

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system_wrappers/source/condition_variable_event_win.cc

Source:

http://www1.cse.wustl.edu/~schmidt/ACE-copying.html

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Files:
system_wrappers/source/set_thread_name_win.h

Source:
http://msdn.microsoft.com/en-us/cc300389.aspx#P

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* /opt/ws_local/PERMITS_SQL/1012932365_1591900514.54/0/listenablefuture-1-0-sources-jar/com/google/common/util/concurrent/ListenableFuture.java

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1.64 racoon 10.0.0

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1.65 tidy 5.6.0

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1.66 e2fsprogs 1.44.4

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Index: tdbsa/tdb.c
===
--- tdbsa.orig/tdb.c
+++ tdbsa/tdb.c
@@ -4,11 +4,11 @@ Rev: 23371
Last Changed Date: 2007-06-06 20:14:06 -0400 (Wed, 06 Jun 2007)
*/
 /*
- Unix SMB/CIFS implementation.
+   trivial database library - standalone version

- trivial database library - private includes
-
- Copyright (C) Andrew Tridgell   2005
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That's all there is to it!
This package was added to the e2fsprogs debian source package by
Theodore Ts'o <tytso@mit.edu> on Sat Mar 15 15:33:37 EST 2003

It is part of the main e2fsprogs distribution, which can be found at:

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Upstream Author: Theodore Ts'o <tytso@mit.edu>

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This is the Debian GNU/Linux prepackaged version of the ss
command-line interface parsing library. It is currently
distributed together with the EXT2 file system utilities, which are
otherwise packaged as "e2fsprogs".

This package was put together by Yann Dirson <dirson@debian.org>,
from sources obtained from a mirror of:
tsx-11.mit.edu:/pub/linux/packages/ext2fs/

From the original distribution:

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#
This is a Makefile stub which handles the creation of BSD shared
libraries.
#
In order to use this stub, the following makefile variables must be defined.
#
BSDLIB_VERSION = 1.0
BSDLIB_IMAGE = libce
BSDLIB_MYDIR = et
BSDLIB_INSTALL_DIR = $(SHLIBDIR)
#

all:: image

real-subdirs:: Makefile
 @echo " MKDIR pic"
 @mkdir -p pic

BSD_LIB = $(BSDLIB_IMAGE).so.$(BSDLIB_VERSION)
BSDLIB_PIC_FLAG = -fpic

```
image:  $(BSD_LIB)

$(BSD_LIB): $(OBJS)
 (cd pic; ld -Bshareable -o $(BSD_LIB) $(LDFLAGS_SHLIB) $(OBJS))
 $(MV) pic/$(BSD_LIB) .
 $(RM) -f ../$(BSD_LIB)
 (cd ..; $(LN) $(LINK_BUILD_FLAGS) \
  `echo $(my_dir) | sed -e 's;lib/;;'`/$(BSD_LIB) $(BSD_LIB))

install-shlibs install:: $(BSD_LIB)
 @echo " INSTALL_PROGRAM $(BSDLIB_INSTALL_DIR)/$(BSD_LIB)"
 @$(INSTALL_PROGRAM) $(BSD_LIB) \
  $(DESTDIR)$(BSDLIB_INSTALL_DIR)/$(BSD_LIB)
 @-$(LDCONFIG)

install-strip: install

install-shlibs-strip: install-shlibs

uninstall-shlibs uninstall::
 $(RM) -f $(DESTDIR)$(BSDLIB_INSTALL_DIR)/$(BSD_LIB)

clean::
 $(RM) -rf pic
 $(RM) -f $(BSD_LIB)
 $(RM) -f ../$(BSD_LIB)
```

This is the Debian GNU/Linux prepackaged version of the Common Error
Description library. It is currently distributed together with the EXT2 file
system utilities, which are otherwise packaged as "e2fsprogs".

This package was put together by Yann Dirson <dirson@debian.org>,
from sources obtained from a mirror of:
tsx-11.mit.edu:/pub/linux/packages/ext2fs/

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Gadi Oxman, August 1995

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1.81 pjnath 2.9

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common_audio/fft4g.c

common_audio/signal_processing/spl_sqrt_floor.c

common_audio/signal_processing/spl_sqrt_floor_arm.S

modules/audio_coding/codecs/g711/main/source/g711.c

modules/audio_coding/codecs/g711/main/source/g711.h

modules/audio_coding/codecs/g722/main/source/g722_decode.c

modules/audio_coding/codecs/g722/main/source/g722_enc_dec.h

modules/audio_coding/codecs/g722/main/source/g722_encode.c

modules/audio_coding/codecs/isac/main/source/fft.c

modules/audio_device/mac/portaudio/pa_memorybarrier.h

modules/audio_device/mac/portaudio/pa_ringbuffer.c

modules/audio_device/mac/portaudio/pa_ringbuffer.h

modules/audio_processing/aec/aec_rdft.c

system_wrappers/source/condition_variable_event_win.cc

system_wrappers/source/set_thread_name_win.h

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//***

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//*

//*   Copyright (c) 1999, Bob Withers - bwit@pobox.com

//*

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//*

//* Enhancements by Stanley Yamane:

//*   o reverse lookup table for the decode function

//*   o reserve string buffer space in advance

//*

//***

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base/md5.h

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/*
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* The algorithm is due to Ron Rivest. This code was
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*

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base/sha1.h

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/*
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* By Steve Reid <sreid@sea-to-sky.net>
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*
* -----------------
* Modified 7/98
* By James H. Brown <jbrown@burgoyne.com>
* Still 100% Public Domain
*

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// sigslot.h: Signal/Slot classes
//
// Written by Sarah Thompson (sarah@telergy.com) 2002.
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common_audio/signal_processing/spl_sqrt_floor_arm.S

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* Written by Wilco Dijkstra, 1996. The following email exchange establishes the

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*
* From: Wilco Dijkstra <Wilco.Dijkstra@ntlworld.com>
* Date: Fri, Jun 24, 2011 at 3:20 AM
* Subject: Re: sqrt routine
* To: Kevin Ma <kma@google.com>
* Hi Kevin,
* Thanks for asking. Those routines are public domain (originally posted to
* comp.sys.arm a long time ago), so you can use them freely for any purpose.
* Cheers,
* Wilco
*
* ----- Original Message -----
* From: "Kevin Ma" <kma@google.com>
* To: <Wilco.Dijkstra@ntlworld.com>
* Sent: Thursday, June 23, 2011 11:44 PM
* Subject: Fwd: sqrt routine
* Hi Wilco,
* I saw your sqrt routine from several web sites, including
* http://www.finesse.demon.co.uk/steven/sqrt.html.
* Just wonder if there's any copyright information with your Successive
* approximation routines, or if I can freely use it for any purpose.
* Thanks.
* Kevin
*/

Files:
modules/audio_coding/codecs/g711/main/source/g711.c
modules/audio_coding/codecs/g711/main/source/g711.h

License:
/*
* SpanDSP - a series of DSP components for telephony
*
* g711.h - In line A-law and u-law conversion routines
*
* Written by Steve Underwood <steveu@coppice.org>
*
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*
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* detriment.
*/

Files:
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modules/audio_coding/codecs/g722/main/source/g722_enc_dec.h
modules/audio_coding/codecs/g722/main/source/g722_encode.c

License:
/*
* SpanDSP - a series of DSP components for telephony
*
* g722_decode.c - The ITU G.722 codec, decode part.
*
* Written by Steve Underwood <steveu@coppice.org>
*
* Copyright (C) 2005 Steve Underwood
*
* Despite my general liking of the GPL, I place my own contributions
* to this code in the public domain for the benefit of all mankind -
* even the slimy ones who might try to proprietize my work and use it
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*
* Based in part on a single channel G.722 codec which is:
*
* Copyright (c) CMU 1993
* Computer Science, Speech Group
* Chengxiang Lu and Alex Hauptmann
*/

Files:
modules/audio_coding/codecs/isac/main/source/fft.c

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modules/audio_device/mac/portaudio/pa_ringbuffer.c
modules/audio_device/mac/portaudio/pa_ringbuffer.h

License:
/*
* Id
* Portable Audio I/O Library
* Memory barrier utilities
*
* Author: Bjorn Roche, XO Audio, LLC
*
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/*
* $Id$
* Portable Audio I/O Library
* Ring Buffer utility.
*
* Author: Phil Burk, http://www.softsynth.com
* modified for SMP safety on Mac OS X by Bjorn Roche
* modified for SMP safety on Linux by Leland Lucius
* also, allowed for const where possible
* modified for multiple-byte-sized data elements by Sven Fischer
*
* Note that this is safe only for a single-thread reader and a
* single-thread writer.
*
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modules/audio_processing/aec/aec_rdft.c

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Source:

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Source:
http://msdn.microsoft.com/en-us/cc300389.aspx#P

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1.82 pjsip 2.9

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base/base64.h

base/md5.cc

base/md5.h

base/sha1.cc

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base/sigslot.cc

base/sigslot.h

common_audio/fft4g.c

common_audio/signal_processing/spl_sqrt_floor.c

common_audio/signal_processing/spl_sqrt_floor_arm.S

modules/audio_coding/codecs/g711/main/source/g711.c

modules/audio_coding/codecs/g711/main/source/g711.h

modules/audio_coding/codecs/g722/main/source/g722_decode.c

modules/audio_coding/codecs/g722/main/source/g722_enc_dec.h

modules/audio_coding/codecs/g722/main/source/g722_encode.c

modules/audio_coding/codecs/isac/main/source/fft.c

modules/audio_device/mac/portaudio/pa_memorybarrier.h

modules/audio_device/mac/portaudio/pa_ringbuffer.c

modules/audio_device/mac/portaudio/pa_ringbuffer.h

modules/audio_processing/aec/aec_rdft.c

system_wrappers/source/condition_variable_event_win.cc

system_wrappers/source/set_thread_name_win.h

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base/base64.h

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//***

//* Base64 - a simple base64 encoder and decoder.

//*

//*   Copyright (c) 1999, Bob Withers - bwit@pobox.com

//*

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//* or commercial, provided the authors copyright notice remains

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//*

//* Enhancements by Stanley Yamane:

//*   o reverse lookup table for the decode function

//*   o reserve string buffer space in advance

//*

//***

Files:

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base/md5.h

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* This code implements the MD5 message-digest algorithm.

* The algorithm is due to Ron Rivest. This code was

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*

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/*

* SHA-1 in C

* By Steve Reid <sreid@sea-to-sky.net>

* 100% Public Domain

*

* -----------------

* Modified 7/98

* By James H. Brown <jbrown@burgoyne.com>

* Still 100% Public Domain

*

Files:

base/sigslot.cc

base/sigslot.h

License:

// sigslot.h: Signal/Slot classes

//

// Written by Sarah Thompson (sarah@telergy.com) 2002.

//

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common_audio/signal_processing/spl_sqrt_floor.c

common_audio/signal_processing/spl_sqrt_floor_arm.S

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```
/*
* Written by Wilco Dijkstra, 1996. The following email exchange establishes the
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*
* From: Wilco Dijkstra <Wilco.Dijkstra@ntlworld.com>
* Date: Fri, Jun 24, 2011 at 3:20 AM
* Subject: Re: sqrt routine
* To: Kevin Ma <kma@google.com>
* Hi Kevin,
* Thanks for asking. Those routines are public domain (originally posted to
* comp.sys.arm a long time ago), so you can use them freely for any purpose.
* Cheers,
* Wilco
*
* ----- Original Message -----
* From: "Kevin Ma" <kma@google.com>
* To: <Wilco.Dijkstra@ntlworld.com>
* Sent: Thursday, June 23, 2011 11:44 PM
* Subject: Fwd: sqrt routine
* Hi Wilco,
* I saw your sqrt routine from several web sites, including
* http://www.finesse.demon.co.uk/steven/sqrt.html.
* Just wonder if there's any copyright information with your Successive
* approximation routines, or if I can freely use it for any purpose.
* Thanks.
* Kevin
*/
```

Files:

modules/audio_coding/codecs/g711/main/source/g711.c

modules/audio_coding/codecs/g711/main/source/g711.h

License:

```
/*
* SpanDSP - a series of DSP components for telephony
*
* g711.h - In line A-law and u-law conversion routines
*
* Written by Steve Underwood <steveu@coppice.org>
*
* Copyright (C) 2001 Steve Underwood
```

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```

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modules/audio_coding/codecs/g722/main/source/g722_decode.c
modules/audio_coding/codecs/g722/main/source/g722_enc_dec.h
modules/audio_coding/codecs/g722/main/source/g722_encode.c

License:
```
/*
 * SpanDSP - a series of DSP components for telephony
 *
 * g722_decode.c - The ITU G.722 codec, decode part.
 *
 * Written by Steve Underwood <steveu@coppice.org>
 *
 * Copyright (C) 2005 Steve Underwood
 *
 *  Despite my general liking of the GPL, I place my own contributions
 *  to this code in the public domain for the benefit of all mankind -
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 *
 * Based in part on a single channel G.722 codec which is:
 *
 * Copyright (c) CMU 1993
 * Computer Science, Speech Group
 * Chengxiang Lu and Alex Hauptmann
 */
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Files:

modules/audio_coding/codecs/isac/main/source/fft.c

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```
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 *    Queen's Univ at Kingston (Canada)
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modules/audio_device/mac/portaudio/pa_ringbuffer.c
modules/audio_device/mac/portaudio/pa_ringbuffer.h

License:
/*
* Id
* Portable Audio I/O Library
* Memory barrier utilities
*
* Author: Bjorn Roche, XO Audio, LLC
*
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*/


/*
* $Id$
* Portable Audio I/O Library
* Ring Buffer utility.
*
* Author: Phil Burk, http://www.softsynth.com
* modified for SMP safety on Mac OS X by Bjorn Roche
* modified for SMP safety on Linux by Leland Lucius
* also, allowed for const where possible
* modified for multiple-byte-sized data elements by Sven Fischer
*
* Note that this is safe only for a single-thread reader and a
* single-thread writer.
*
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```

Files:

common_audio/fft4g.c

modules/audio_processing/aec/aec_rdft.c

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```
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*/
```

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system_wrappers/source/condition_variable_event_win.cc

Source:

http://www1.cse.wustl.edu/~schmidt/ACE-copying.html

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The source code for a work means the preferred form of the work for
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  in the event an application does not supply such function or
  table, the facility still operates, and performs whatever part of
  its purpose remains meaningful.

  (For example, a function in a library to compute square roots has
  a purpose that is entirely well-defined independent of the
  application. Therefore, Subsection 2d requires that any
  application-supplied function or table used by this function must

be optional: if the application does not supply it, the square
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medium customarily used for software interchange.

 If distribution of object code is made by offering access to copy

from a designated place, then offering equivalent access to copy the
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   with the Library, with the complete machine-readable "work that
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1.84 libevent 2.1.8

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1.88 zlib 1.2.11

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The data format used by the zlib library is described by RFCs (Request for
Comments) 1950 to 1952 in the files http://tools.ietf.org/html/rfc1950
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*/

1.89 ldns 1.10.0

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1.90 simple 2.6.2

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1.91 angle 2.1

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1.92 lz4 1.8.3

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1.93 nanohttpd 2.2.0

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1.94 zlib 1.2.3

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/* zlib.h -- interface of the 'zlib' general purpose compression library
version 1.1.4, March 11th, 2002

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Jean-loup Gailly   Mark Adler
jloup@gzip.org   madler@alumni.caltech.edu

The data format used by the zlib library is described by RFCs (Request for
Comments) 1950 to 1952 in the files ftp://ds.internic.net/rfc/rfc1950.txt
(zlib format), rfc1951.txt (deflate format) and rfc1952.txt (gzip format).
*/
/* match.s -- Pentium-optimized version of longest_match()
* Written for zlib 1.1.2
* Copyright (C) 1998 Brian Raiter <breadbox@muppetlabs.com>
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*/

1.95 libilbc 2.0.2

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1.96 json-cpp 1.9.1

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1.97 llvm 3.9

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```
; RUN: llc < %s -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
;
; Test that early if conversion produces LOCR with operands of the right
; register classes.

define void @autogen_SD4739(i8*) {
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
 %L34 = load i8, i8* %0
 %Cmp56 = icmp sgt i8 undef, %L34
 br label %CF246

CF246:                             ; preds = %CF246, %BB
 %Sl163 = select i1 %Cmp56, i8 %L34, i8 undef
 br i1 undef, label %CF246, label %CF248

CF248:                             ; preds = %CF248, %CF246
 store i8 %Sl163, i8* %0
 br label %CF248
}
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=avx512vl,avx512bw,avx512dq,prefer-256-bit |
FileCheck %s
```

; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

```
define void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" {
; CHECK-LABEL: add256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vpaddd (%rsi), %ymm0, %ymm0
; CHECK-NEXT:    vpaddd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:    vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:    vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %d = load <16 x i32>, <16 x i32>* %a
  %e = load <16 x i32>, <16 x i32>* %b
  %f = add <16 x i32> %d, %e
  store <16 x i32> %f, <16 x i32>* %c
  ret void
}

define void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="512" {
; CHECK-LABEL: add512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:    vpaddd (%rsi), %zmm0, %zmm0
; CHECK-NEXT:    vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %d = load <16 x i32>, <16 x i32>* %a
  %e = load <16 x i32>, <16 x i32>* %b
  %f = add <16 x i32> %d, %e
  store <16 x i32> %f, <16 x i32>* %c
  ret void
}

define void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" {
; CHECK-LABEL: avg_v64i8_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rsi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT:    vpavgb (%rdi), %ymm0, %ymm0
; CHECK-NEXT:    vpavgb 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT:    vmovdqu %ymm1, (%rax)
; CHECK-NEXT:    vmovdqu %ymm0, (%rax)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %1 = load <64 x i8>, <64 x i8>* %a
```

```
%2 = load <64 x i8>, <64 x i8>* %b
%3 = zext <64 x i8> %1 to <64 x i32>
%4 = zext <64 x i8> %2 to <64 x i32>
%5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%6 = add nuw nsw <64 x i32> %5, %4
%7 = lshr <64 x i32> %6, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%8 = trunc <64 x i32> %7 to <64 x i8>
store <64 x i8> %8, <64 x i8>* undef, align 4
ret void
}


define void @avg_v64i8_512(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="512" {
; CHECK-LABEL: avg_v64i8_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rsi), %zmm0
; CHECK-NEXT:    vpavgb (%rdi), %zmm0, %zmm0
; CHECK-NEXT:    vmovdqu64 %zmm0, (%rax)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%1 = load <64 x i8>, <64 x i8>* %a
%2 = load <64 x i8>, <64 x i8>* %b
%3 = zext <64 x i8> %1 to <64 x i32>
%4 = zext <64 x i8> %2 to <64 x i32>
%5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%6 = add nuw nsw <64 x i32> %5, %4
%7 = lshr <64 x i32> %6, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
%8 = trunc <64 x i32> %7 to <64 x i8>
store <64 x i8> %8, <64 x i8>* undef, align 4
ret void
}

define void @pmaddwd_32_256(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-
width"="256" {
; CHECK-LABEL: pmaddwd_32_256:
; CHECK:       # %bb.0:
```

```
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vpmaddwd (%rsi), %ymm0, %ymm0
; CHECK-NEXT:    vpmaddwd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:    vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:    vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %A = load <32 x i16>, <32 x i16>* %APtr
  %B = load <32 x i16>, <32 x i16>* %BPtr
  %a = sext <32 x i16> %A to <32 x i32>
  %b = sext <32 x i16> %B to <32 x i32>
  %m = mul nsw <32 x i32> %a, %b
  %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
  %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32
13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
  %ret = add <16 x i32> %odd, %even
  store <16 x i32> %ret, <16 x i32>* %CPtr
  ret void
}

define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-
width"="512" {
; CHECK-LABEL: pmaddwd_32_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:    vpmaddwd (%rsi), %zmm0, %zmm0
; CHECK-NEXT:    vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %A = load <32 x i16>, <32 x i16>* %APtr
  %B = load <32 x i16>, <32 x i16>* %BPtr
  %a = sext <32 x i16> %A to <32 x i32>
  %b = sext <32 x i16> %B to <32 x i32>
  %m = mul nsw <32 x i32> %a, %b
  %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
  %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32
13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
  %ret = add <16 x i32> %odd, %even
  store <16 x i32> %ret, <16 x i32>* %CPtr
  ret void
}

define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-
width"="256" {
; CHECK-LABEL: psubus_64i8_max_256:
```

```
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vpsubusb (%rsi), %ymm0, %ymm0
; CHECK-NEXT:    vpsubusb 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:    vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:    vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %x = load <64 x i8>, <64 x i8>* %xptr
  %y = load <64 x i8>, <64 x i8>* %yptr
  %cmp = icmp ult <64 x i8> %x, %y
  %max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
  %res = sub <64 x i8> %max, %y
  store <64 x i8> %res, <64 x i8>* %zptr
  ret void
}

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-width"="512" {
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:    vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT:    vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %x = load <64 x i8>, <64 x i8>* %xptr
  %y = load <64 x i8>, <64 x i8>* %yptr
  %cmp = icmp ult <64 x i8> %x, %y
  %max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
  %res = sub <64 x i8> %max, %y
  store <64 x i8> %res, <64 x i8>* %zptr
  ret void
}

define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
; CHECK-LABEL: _Z9test_charPcS_i_256:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    movl %edx, %eax
; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:    xorl %ecx, %ecx
; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:    vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB8_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
```

```
; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %ymm3
; CHECK-NEXT:    vpmovsxbw 16(%rdi,%rcx), %ymm4
; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %ymm5
; CHECK-NEXT:    vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-NEXT:    vpaddd %ymm1, %ymm3, %ymm1
; CHECK-NEXT:    vpmovsxbw 16(%rsi,%rcx), %ymm3
; CHECK-NEXT:    vpmaddwd %ymm4, %ymm3, %ymm3
; CHECK-NEXT:    vpaddd %ymm2, %ymm3, %ymm2
; CHECK-NEXT:    addq $32, %rcx
; CHECK-NEXT:    cmpq %rcx, %rax
; CHECK-NEXT:    jne .LBB8_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm1
; CHECK-NEXT:    vpaddd %ymm0, %ymm2, %ymm0
; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:    vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vmovd %xmm0, %eax
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
entry:
 %3 = zext i32 %2 to i64
 br label %vector.body


vector.body:
 %index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
 %vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
 %4 = getelementptr inbounds i8, i8* %0, i64 %index
 %5 = bitcast i8* %4 to <32 x i8>*
 %wide.load = load <32 x i8>, <32 x i8>* %5, align 1
 %6 = sext <32 x i8> %wide.load to <32 x i32>
 %7 = getelementptr inbounds i8, i8* %1, i64 %index
 %8 = bitcast i8* %7 to <32 x i8>*
 %wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
 %9 = sext <32 x i8> %wide.load14 to <32 x i32>
 %10 = mul nsw <32 x i32> %9, %6
 %11 = add nsw <32 x i32> %10, %vec.phi
 %index.next = add i64 %index, 32
 %12 = icmp eq i64 %index.next, %3
 br i1 %12, label %middle.block, label %vector.body


middle.block:
 %rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
 i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
```

i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
 %rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef>
 %bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
 %rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef>
 %bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
 %rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef>
 %bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
 %rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef>
 %bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
 %13 = extractelement <32 x i32> %bin.rdx20, i32 0
 ret i32 %13
}

define i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="512" {
; CHECK-LABEL: _Z9test_charPcS_i_512:
; CHECK: # %bb.0: # %entry
; CHECK-NEXT: movl %edx, %eax
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: xorl %ecx, %ecx
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB9_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-NEXT: vpmovsxbw (%rsi,%rcx), %zmm3
; CHECK-NEXT: vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-NEXT: vpaddd %zmm1, %zmm2, %zmm1
; CHECK-NEXT: addq $32, %rcx
; CHECK-NEXT: cmpq %rcx, %rax
; CHECK-NEXT: jne .LBB9_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT: vpaddd %zmm0, %zmm1, %zmm0
; CHECK-NEXT: vextracti64x4 $1, %zmm0, %ymm1

; CHECK-NEXT: vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT: vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vmovd %xmm0, %eax
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
 %3 = zext i32 %2 to i64
 br label %vector.body

vector.body:
 %index = phi i64 [%index.next, %vector.body], [0, %entry]
 %vec.phi = phi <32 x i32> [%11, %vector.body], [zeroinitializer, %entry]
 %4 = getelementptr inbounds i8, i8* %0, i64 %index
 %5 = bitcast i8* %4 to <32 x i8>*
 %wide.load = load <32 x i8>, <32 x i8>* %5, align 1
 %6 = sext <32 x i8> %wide.load to <32 x i32>
 %7 = getelementptr inbounds i8, i8* %1, i64 %index
 %8 = bitcast i8* %7 to <32 x i8>*
 %wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
 %9 = sext <32 x i8> %wide.load14 to <32 x i32>
 %10 = mul nsw <32 x i32> %9, %6
 %11 = add nsw <32 x i32> %10, %vec.phi
 %index.next = add i64 %index, 32
 %12 = icmp eq i64 %index.next, %3
 br i1 %12, label %middle.block, label %vector.body

middle.block:
 %rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef>
 %bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
 %rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
 %rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
 %rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32

undef, i32 undef>
  %bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
  %rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef>
  %bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
  %13 = extractelement <32 x i32> %bin.rdx20, i32 0
  ret i32 %13
}

@a = global [1024 x i8] zeroinitializer, align 16
@b = global [1024 x i8] zeroinitializer, align 16

define i32 @sad_16i8_256() "min-legal-vector-width"="256" {
; CHECK-LABEL: sad_16i8_256:
; CHECK: # %bb.0: # %entry
; CHECK-NEXT: vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT: movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT: vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT: .p2align 4, 0x90
; CHECK-NEXT: .LBB10_1: # %vector.body
; CHECK-NEXT: # =>This Inner Loop Header: Depth=1
; CHECK-NEXT: vmovdqu a+1024(%rax), %xmm2
; CHECK-NEXT: vpsadbw b+1024(%rax), %xmm2, %xmm2
; CHECK-NEXT: vpaddd %ymm1, %ymm2, %ymm1
; CHECK-NEXT: addq $4, %rax
; CHECK-NEXT: jne .LBB10_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT: vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT: vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT: vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT: vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT: vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT: vmovd %xmm0, %eax
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
entry:
  br label %vector.body

vector.body:
  %index = phi i64 [0, %entry], [%index.next, %vector.body]
  %vec.phi = phi <16 x i32> [zeroinitializer, %entry], [%10, %vector.body]
  %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index

```
%1 = bitcast i8* %0 to <16 x i8>*
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
%2 = zext <16 x i8> %wide.load to <16 x i32>
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
%4 = bitcast i8* %3 to <16 x i8>*
%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
%6 = sub nsw <16 x i32> %2, %5
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

middle.block:
%.lcssa = phi <16 x i32> [ %10, %vector.body ]
%rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define i32 @sad_16i8_512() "min-legal-vector-width"="512" {
; CHECK-LABEL: sad_16i8_512:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:    movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB11_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:    vmovdqu a+1024(%rax), %xmm1
; CHECK-NEXT:    vpsadbw b+1024(%rax), %xmm1, %xmm1
```

```
; CHECK-NEXT:    vpaddd %zmm0, %zmm1, %zmm0
; CHECK-NEXT:    addq $4, %rax
; CHECK-NEXT:    jne .LBB11_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vmovd %xmm0, %eax
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
entry:
 br label %vector.body

vector.body:
 %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
 %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
 %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
 %1 = bitcast i8* %0 to <16 x i8>*
 %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
 %2 = zext <16 x i8> %wide.load to <16 x i32>
 %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
 %4 = bitcast i8* %3 to <16 x i8>*
 %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
 %5 = zext <16 x i8> %wide.load1 to <16 x i32>
 %6 = sub nsw <16 x i32> %2, %5
 %7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -
1, i32 -1, i32 -1, i32 -1, i32 -1>
 %8 = sub nsw <16 x i32> zeroinitializer, %6
 %9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
 %10 = add nsw <16 x i32> %9, %vec.phi
 %index.next = add i64 %index, 4
 %11 = icmp eq i64 %index.next, 1024
 br i1 %11, label %middle.block, label %vector.body

middle.block:
 %.lcssa = phi <16 x i32> [ %10, %vector.body ]
 %rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12,
i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
 %rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef>
 %bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
```

```
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}


define void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm1
; CHECK-NEXT:    vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT:    vmovaps %ymm1, (%rdi)
; CHECK-NEXT:    vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}


define void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
}


define void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f64_256:
```

```
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT:    vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT:    vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT:    vmovaps %ymm3, (%rdi)
; CHECK-NEXT:    vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT:    vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = sitofp <16 x i1> %mask to <16 x double>
  store <16 x double> %1, <16 x double>* %res
  ret void
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f64_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:    vmovaps %zmm1, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = sitofp <16 x i1> %mask to <16 x double>
  store <16 x double> %1, <16 x double>* %res
  ret void
}

define void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f32_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vpsrld $31, %ymm0, %ymm0
```

```
; CHECK-NEXT:    vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm1
; CHECK-NEXT:    vpsrld $31, %ymm1, %ymm1
; CHECK-NEXT:    vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT:    vmovaps %ymm1, (%rdi)
; CHECK-NEXT:    vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = uitofp <16 x i1> %mask to <16 x float>
  store <16 x float> %1, <16 x float>* %res
  ret void
}

define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f32_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT:    vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = uitofp <16 x i1> %mask to <16 x float>
  store <16 x float> %1, <16 x float>* %res
  ret void
}

define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f64_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm2
; CHECK-NEXT:    vpsrld $31, %ymm2, %ymm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT:    vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT:    vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT:    vmovaps %ymm3, (%rdi)
; CHECK-NEXT:    vmovaps %ymm0, 96(%rdi)
```

```
; CHECK-NEXT:    vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %mask = icmp slt <16 x i16> %a, zeroinitializer
 %1 = uitofp <16 x i1> %mask to <16 x double>
 store <16 x double> %1, <16 x double>* %res
 ret void
}

define void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f64_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:    vmovaps %zmm1, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %mask = icmp slt <16 x i16> %a, zeroinitializer
 %1 = uitofp <16 x i1> %mask to <16 x double>
 store <16 x double> %1, <16 x double>* %res
 ret void
}

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-width"="256" {
; CHECK-LABEL: test_16f32toub_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:    vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:    vpmovd2m %ymm1, %k0
; CHECK-NEXT:    vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:    vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:    vpmovd2m %ymm1, %k1
; CHECK-NEXT:    kunpckbw %k0, %k1, %k1
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:    retq
 %a = load <16 x float>, <16 x float>* %ptr
 %mask = fptoui <16 x float> %a to <16 x i1>
 %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
 ret <16 x i16> %select
}

define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
```

```
width"="512" {
; CHECK-LABEL: test_16f32toub_512:
; CHECK:      # %bb.0:
; CHECK-NEXT:   vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:   vpslld $31, %zmm1, %zmm1
; CHECK-NEXT:   vpmovd2m %zmm1, %k1
; CHECK-NEXT:   vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:   retq
 %a = load <16 x float>, <16 x float>* %ptr
 %mask = fptoui <16 x float> %a to <16 x i1>
 %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
 ret <16 x i16> %select
}


define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="256" {
; CHECK-LABEL: test_16f32tosb_256:
; CHECK:      # %bb.0:
; CHECK-NEXT:   vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:   vpmovd2m %ymm1, %k0
; CHECK-NEXT:   vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:   vpmovd2m %ymm1, %k1
; CHECK-NEXT:   kunpckbw %k0, %k1, %k1
; CHECK-NEXT:   vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:   retq
 %a = load <16 x float>, <16 x float>* %ptr
 %mask = fptosi <16 x float> %a to <16 x i1>
 %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
 ret <16 x i16> %select
}


define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {
; CHECK-LABEL: test_16f32tosb_512:
; CHECK:      # %bb.0:
; CHECK-NEXT:   vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:   vpmovd2m %zmm1, %k1
; CHECK-NEXT:   vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:   retq
 %a = load <16 x float>, <16 x float>* %ptr
 %mask = fptosi <16 x float> %a to <16 x i1>
 %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
 ret <16 x i16> %select
}


define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
; CHECK-LABEL: mul256:
; CHECK:      # %bb.0:
```

; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm2[8],ymm0[8],ymm2[9],ymm0[9],ymm2[10],ymm0[10],ymm2[11],ymm0[11],ymm2[12],ymm0[12],ymm2[13],ymm0[13],ymm2[14],ymm0[14],ymm2[15],ymm0[15],ymm2[24],ymm0[24],ymm2[25],ymm0[25],ymm2[26],ymm0[26],ymm2[27],ymm0[27],ymm2[28],ymm0[28],ymm2[29],ymm0[29],ymm2[30],ymm0[30],ymm2[31],ymm0[31]
; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm5 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-NEXT: vmovdqa {{.*#+}} ymm5 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255]
; CHECK-NEXT: vpand %ymm5, %ymm4, %ymm4
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm2 =
ymm2[0],ymm0[0],ymm2[1],ymm0[1],ymm2[2],ymm0[2],ymm2[3],ymm0[3],ymm2[4],ymm0[4],ymm2[5],ymm0[5],ymm2[6],ymm0[6],ymm2[7],ymm0[7],ymm2[16],ymm0[16],ymm2[17],ymm0[17],ymm2[18],ymm0[18],ymm2[19],ymm0[19],ymm2[20],ymm0[20],ymm2[21],ymm0[21],ymm2[22],ymm0[22],ymm2[23],ymm0[23]
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-NEXT: vpmullw %ymm2, %ymm0, %ymm0
; CHECK-NEXT: vpand %ymm5, %ymm0, %ymm0
; CHECK-NEXT: vpackuswb %ymm4, %ymm0, %ymm0
; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm2 =
ymm3[8],ymm0[8],ymm3[9],ymm0[9],ymm3[10],ymm0[10],ymm3[11],ymm0[11],ymm3[12],ymm0[12],ymm3[13],ymm0[13],ymm3[14],ymm0[14],ymm3[15],ymm0[15],ymm3[24],ymm0[24],ymm3[25],ymm0[25],ymm3[26],ymm0[26],ymm3[27],ymm0[27],ymm3[28],ymm0[28],ymm3[29],ymm0[29],ymm3[30],ymm0[30],ymm3[31],ymm0[31]
; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm1[8],ymm0[8],ymm1[9],ymm0[9],ymm1[10],ymm0[10],ymm1[11],ymm0[11],ymm1[12],ymm0[12],ymm1[13],ymm0[13],ymm1[14],ymm0[14],ymm1[15],ymm0[15],ymm1[24],ymm0[24],ymm1[25],ymm0[25],ymm1[26],ymm0[26],ymm1[27],ymm0[27],ymm1[28],ymm0[28],ymm1[29],ymm0[29],ymm1[30],ymm0[30],ymm1[31],ymm0[31]
; CHECK-NEXT: vpmullw %ymm2, %ymm4, %ymm2
; CHECK-NEXT: vpand %ymm5, %ymm2, %ymm2
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm3 =
ymm3[0],ymm0[0],ymm3[1],ymm0[1],ymm3[2],ymm0[2],ymm3[3],ymm0[3],ymm3[4],ymm0[4],ymm3[5],ymm0[5],ymm3[6],ymm0[6],ymm3[7],ymm0[7],ymm3[16],ymm0[16],ymm3[17],ymm0[17],ymm3[18],ymm0[18],ymm3[19],ymm0[19],ymm3[20],ymm0[20],ymm3[21],ymm0[21],ymm3[22],ymm0[22],ymm3[23],ymm0[23]
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm1 =
ymm1[0],ymm0[0],ymm1[1],ymm0[1],ymm1[2],ymm0[2],ymm1[3],ymm0[3],ymm1[4],ymm0[4],ymm1[5],ymm0[5],ymm1[6],ymm0[6],ymm1[7],ymm0[7],ymm1[16],ymm0[16],ymm1[17],ymm0[17],ymm1[18],ymm0[18],ymm1[19],ymm0[19],ymm1[20],ymm0[20],ymm1[21],ymm0[21],ymm1[22],ymm0[22],ymm1[23],ymm0[23]
; CHECK-NEXT: vpmullw %ymm3, %ymm1, %ymm1
; CHECK-NEXT: vpand %ymm5, %ymm1, %ymm1
; CHECK-NEXT: vpackuswb %ymm2, %ymm1, %ymm1
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)

```
; CHECK-NEXT:    vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %d = load <64 x i8>, <64 x i8>* %a
  %e = load <64 x i8>, <64 x i8>* %b
  %f = mul <64 x i8> %d, %e
  store <64 x i8> %f, <64 x i8>* %c
  ret void
}

define void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" {
; CHECK-LABEL: mul512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:    vmovdqa64 (%rsi), %zmm1
; CHECK-NEXT:    vpunpckhbw {{.*#+}} zmm2 =
zmm1[8],zmm0[8],zmm1[9],zmm0[9],zmm1[10],zmm0[10],zmm1[11],zmm0[11],zmm1[12],zmm0[12],zmm1[13],
zmm0[13],zmm1[14],zmm0[14],zmm1[15],zmm0[15],zmm1[24],zmm0[24],zmm1[25],zmm0[25],zmm1[26],zmm0
[26],zmm1[27],zmm0[27],zmm1[28],zmm0[28],zmm1[29],zmm0[29],zmm1[30],zmm0[30],zmm1[31],zmm0[31],z
mm1[40],zmm0[40],zmm1[41],zmm0[41],zmm1[42],zmm0[42],zmm1[43],zmm0[43],zmm1[44],zmm0[44],zmm1[
45],zmm0[45],zmm1[46],zmm0[46],zmm1[47],zmm0[47],zmm1[56],zmm0[56],zmm1[57],zmm0[57],zmm1[58],z
mm0[58],zmm1[59],zmm0[59],zmm1[60],zmm0[60],zmm1[61],zmm0[61],zmm1[62],zmm0[62],zmm1[63],zmm0[
63]
; CHECK-NEXT:    vpunpckhbw {{.*#+}} zmm3 =
zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-NEXT:    vpmullw %zmm2, %zmm3, %zmm2
; CHECK-NEXT:    vmovdqa64 {{.*#+}} zmm3 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,2
55,255,255,255,255,255]
; CHECK-NEXT:    vpandq %zmm3, %zmm2, %zmm2
; CHECK-NEXT:    vpunpcklbw {{.*#+}} zmm1 =
zmm1[0],zmm0[0],zmm1[1],zmm0[1],zmm1[2],zmm0[2],zmm1[3],zmm0[3],zmm1[4],zmm0[4],zmm1[5],zmm0[5]
,zmm1[6],zmm0[6],zmm1[7],zmm0[7],zmm1[16],zmm0[16],zmm1[17],zmm0[17],zmm1[18],zmm0[18],zmm1[19]
,zmm0[19],zmm1[20],zmm0[20],zmm1[21],zmm0[21],zmm1[22],zmm0[22],zmm1[23],zmm0[23],zmm1[32],zmm
0[32],zmm1[33],zmm0[33],zmm1[34],zmm0[34],zmm1[35],zmm0[35],zmm1[36],zmm0[36],zmm1[37],zmm0[37],
zmm1[38],zmm0[38],zmm1[39],zmm0[39],zmm1[48],zmm0[48],zmm1[49],zmm0[49],zmm1[50],zmm0[50],zmm1
[51],zmm0[51],zmm1[52],zmm0[52],zmm1[53],zmm0[53],zmm1[54],zmm0[54],zmm1[55],zmm0[55]
; CHECK-NEXT:    vpunpcklbw {{.*#+}} zmm0 =
zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-NEXT:    vpmullw %zmm1, %zmm0, %zmm0
; CHECK-NEXT:    vpandq %zmm3, %zmm0, %zmm0
; CHECK-NEXT:    vpackuswb %zmm2, %zmm0, %zmm0
; CHECK-NEXT:    vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %d = load <64 x i8>, <64 x i8>* %a
```

```
  %e = load <64 x i8>, <64 x i8>* %b
  %f = mul <64 x i8> %d, %e
  store <64 x i8> %f, <64 x i8>* %c
  ret void
}
```
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Program   Directory
-------   ---------
<none yet>
; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=CHECK,VEC256,AVX
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -
mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-
prefixes=CHECK,VEC256,SKX256
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -
mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512

define void @zext256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'zext256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x

i32>

; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; VEC512-LABEL: 'zext256'

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

 %A = zext <8 x i16> undef to <8 x i64>

 %B = zext <8 x i32> undef to <8 x i64>

 %C = zext <16 x i8> undef to <16 x i32>

 %D = zext <16 x i16> undef to <16 x i32>

 %E = zext <32 x i8> undef to <32 x i16>

 ret void

}

define void @zext512() "min-legal-vector-width"="512" {

; AVX-LABEL: 'zext512'

; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; SKX256-LABEL: 'zext512'

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;
; VEC512-LABEL: 'zext512'
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
 %A = zext <8 x i16> undef to <8 x i64>
 %B = zext <8 x i32> undef to <8 x i64>
 %C = zext <16 x i8> undef to <16 x i32>
 %D = zext <16 x i16> undef to <16 x i32>
 %E = zext <32 x i8> undef to <32 x i16>
 ret void
}

define void @sext256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'sext256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'sext256'
; VEC512-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
 %A = sext <8 x i8> undef to <8 x i64>
 %B = sext <8 x i16> undef to <8 x i64>
 %C = sext <8 x i32> undef to <8 x i64>
 %D = sext <16 x i8> undef to <16 x i32>
 %E = sext <16 x i16> undef to <16 x i32>
 %F = sext <32 x i8> undef to <32 x i16>
 ret void
}

define void @sext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'sext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'sext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'sext512'
; VEC512-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x

i32>

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

 %A = sext <8 x i8> undef to <8 x i64>

 %B = sext <8 x i16> undef to <8 x i64>

 %C = sext <8 x i32> undef to <8 x i64>

 %D = sext <16 x i8> undef to <16 x i32>

 %E = sext <16 x i16> undef to <16 x i32>

 %F = sext <32 x i8> undef to <32 x i16>

 ret void

}

$OpenBSD: COPYRIGHT,v 1.3 2003/06/02 20:18:36 millert Exp $

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=-=
/*-
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```
; RUN: llc -march=hexagon < %s
; REQUIRES: asserts

; The two loads based on %struct.0, loading two different data types
; cause LSR to assume type "void" for the memory type. This would then
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"

%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }

define hidden fastcc void @fred() unnamed_addr #0 {
entry:
 br i1 undef, label %while.end, label %while.body.lr.ph

while.body.lr.ph:                    ; preds = %entry
 br label %while.body

while.body:                          ; preds = %exit.2, %while.body.lr.ph
 %lsr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
 switch i32 undef, label %exit [
   i32 1, label %sw.bb.i
   i32 2, label %sw.bb3.i
 ]

sw.bb.i:                             ; preds = %while.body
 unreachable
```

```
sw.bb3.i:                              ; preds = %while.body
 unreachable

exit:                                  ; preds = %while.body
 switch i32 undef, label %exit.2 [
  i32 1, label %sw.bb.i17
  i32 2, label %sw.bb3.i20
 ]

sw.bb.i17:                             ; preds = %.exit
 %0 = bitcast %struct.0* %lsr.iv to i32*
 %1 = load i32, i32* %0, align 4
 unreachable

sw.bb3.i20:                            ; preds = %exit
 %2 = bitcast %struct.0* %lsr.iv to i8**
 %3 = load i8*, i8** %2, align 4
 unreachable

exit.2:                                ; preds = %exit
 %cgep22 = getelementptr %struct.0, %struct.0* %lsr.iv, i32 1
 br label %while.body

while.end:                             ; preds = %entry
 ret void
}

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }
; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s

define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
; CHECK-LABEL: test_sitofp_fixed:

 ; First, extend each i32 to i64
; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0
; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0

 ; Next, convert each to double.
; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
```

```
; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]

; CHECK: ret
 %flt = sitofp <16 x i32> %in to <16 x double>
 %res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0,
double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0,
double 64.0>
 ret <16 x double> %res
}

; This one is small enough to satisfy isSimple, but still illegally large.
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:

; CHECK-DAG: scvtf.2d v0, v0
; CHECK-DAG: scvtf.2d v1, v1

; CHECK: ret
 %flt = sitofp <4 x i64> %in to <4 x double>
 %res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
 ret <4 x double> %res
}
; RUN: opt %s -inline -S | FileCheck %s

define internal void @innerSmall() "min-legal-vector-width"="128" {
 ret void
}

define internal void @innerLarge() "min-legal-vector-width"="512" {
 ret void
}

define internal void @innerNoAttribute() {
 ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.
define void @outerNoAttribute() {
 call void @innerLarge()
 ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
```

```
  call void @innerLarge()
  ret void
}

define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
  call void @innerSmall()
  ret void
}

; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
  call void @innerNoAttribute()
  ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }
```

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```
; RUN: opt -consthoist -S -o - %s | FileCheck %s
target datalayout = "e-m:e-p:32:32-i64:64-v128:64:128-a:0:32-n32-S64"
target triple = "thumbv6m-none--musleabi"


; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
; CHECK: foo_i8
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874720 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK-DAG: %[[C3:const[0-9]?]] = bitcast i32 805873720 to i32
; CHECK-DAG: %[[C4:const[0-9]?]] = bitcast i32 805873688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i8*
; CHECK-NEXT: %1 = load volatile i8, i8* %0
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i8*
; CHECK-NEXT: %3 = load volatile i8, i8* %2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 31
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i8*
; CHECK-NEXT: %5 = load volatile i8, i8* %4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i8*
; CHECK-NEXT: %7 = load volatile i8, i8* %6
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 7
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i8*
; CHECK-NEXT: %9 = load volatile i8, i8* %8
; CHECK-NEXT: %10 = inttoptr i32 %[[C4]] to i8*
; CHECK-NEXT: store i8 %9, i8* %10
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C4]], 31
; CHECK-NEXT: %11 = inttoptr i32 %[[M4]] to i8*
; CHECK-NEXT: store i8 %7, i8* %11
; CHECK-NEXT: %12 = inttoptr i32 %[[C3]] to i8*
; CHECK-NEXT: store i8 %5, i8* %12
; CHECK-NEXT: %[[M5:const_mat[0-9]?]] = add i32 %[[C3]], 7
; CHECK-NEXT: %13 = inttoptr i32 %[[M5]] to i8*
; CHECK-NEXT: store i8 %3, i8* %13
; CHECK-NEXT: %[[M6:const_mat[0-9]?]] = add i32 %[[C1]], 80
; CHECK-NEXT: %14 = inttoptr i32 %[[M6]] to i8*
; CHECK-NEXT: store i8* %14, i8** @goo

@goo = global i8* undef

define void @foo_i8() {
entry:
 %0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
 %1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
 %2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
 %3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
```

```
%4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
store i8 %4, i8* inttoptr(i32 805873688 to i8*)
store i8 %3, i8* inttoptr(i32 805873719 to i8*)
store i8 %2, i8* inttoptr(i32 805873720 to i8*)
store i8 %1, i8* inttoptr(i32 805873727 to i8*)
store i8* inttoptr(i32 805874800 to i8*), i8** @goo
ret void
}
```

; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 22
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %11 = load volatile i16, i16* %10, align 2

```
define void @foo_i16() {
entry:
%0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
%1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
%2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
%3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
%4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
%5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
ret void
}
```

; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4

```
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i32*
; CHECK-NEXT: %3 = load volatile i32, i32* %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 124
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i32*
; CHECK-NEXT: %5 = load volatile i32, i32* %4, align 4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i32*
; CHECK-NEXT: %7 = load volatile i32, i32* %6, align 4
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 8
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i32*
; CHECK-NEXT: %9 = load volatile i32, i32* %8, align 4
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 12
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i32*
; CHECK-NEXT: %11 = load volatile i32, i32* %10, align 4


define void @foo_i32() {
entry:
 %0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
 %1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
 %2 = load volatile i32, i32* inttoptr (i32 805874812 to i32*), align 4
 %3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
 %4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
 %5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
 ret void
}
```

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```
; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s
;
; D31946
; Check that we dont end up with the ""LLVM ERROR: Cannot select" error.
; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128, fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) {
 %cmp = fcmp ogt fp128 %a, %b
 %sub = fsub fp128 %a, %b
 %res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000
 ret fp128 %res
; CHECK-LABEL: TestSelect:
; CHECK       movaps 16(%rsp), %xmm1
; CHECK-NEXT  callq __subtf3
; CHECK-NEXT  testl %ebx, %ebx
; CHECK-NEXT  jg .LBB0_2
; CHECK-NEXT # %bb.1:
; CHECK-NEXT  movaps .LCPI0_0(%rip), %xmm0
; CHECK-NEXT .LBB0_2:
; CHECK-NEXT  addq $32, %rsp
; CHECK-NEXT  popq %rbx
; CHECK-NEXT  retq
}

define fp128 @TestFabs(fp128 %a) {
 %res = call fp128 @llvm.fabs.f128(fp128 %a)
```

```
 ret fp128 %res
; CHECK-LABEL: TestFabs:
; CHECK      andps .LCPI1_0(%rip), %xmm0
; CHECK-NEXT retq
}

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
 %res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
 ret fp128 %res
; CHECK-LABEL: TestCopysign:
; CHECK      andps .LCPI2_1(%rip), %xmm0
; CHECK-NEXT orps %xmm1, %xmm0
; CHECK-NEXT retq
}

define fp128 @TestFneg(fp128 %a) {
 %mul = fmul fp128 %a, %a
 %res = fsub fp128 0xL00000000000000008000000000000000, %mul
 ret fp128 %res
; CHECK-LABEL: TestFneg:
; CHECK      movaps %xmm0, %xmm1
; CHECK-NEXT callq __multf3
; CHECK-NEXT xorps .LCPI3_0(%rip), %xmm0
; CHECK-NEXT popq %rax
; CHECK-NEXT retq
}
```
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Python was created in the early 1990s by Guido van Rossum at Stichting
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as a successor of a language called ABC. Guido remains Python's
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In 1995, Guido continued his work on Python at the Corporation for
National Research Initiatives (CNRI, see http://www.cnri.reston.va.us)
in Reston, Virginia where he released several versions of the
software.

In May 2000, Guido and the Python core development team moved to
BeOpen.com to form the BeOpen PythonLabs team. In October of the same
year, the PythonLabs team moved to Digital Creations, which became
Zope Corporation. In 2001, the Python Software Foundation (PSF, see
https://www.python.org/psf/) was formed, a non-profit organization
created specifically to own Python-related Intellectual Property.
Zope Corporation was a sponsoring member of the PSF.

All Python releases are Open Source (see http://www.opensource.org for
the Open Source Definition). Historically, most, but not all, Python
releases have also been GPL-compatible; the table below summarizes
the various releases.

Release	Derived from	Year	Owner	GPL-compatible? (1)
0.9.0 thru 1.2		1991-1995	CWI	yes
1.3 thru 1.5.2	1.2	1995-1999	CNRI	yes
1.6	1.5.2	2000	CNRI	no
2.0	1.6	2000	BeOpen.com	no
1.6.1	1.6	2001	CNRI	yes (2)
2.1	2.0+1.6.1	2001	PSF	no
2.0.1	2.0+1.6.1	2001	PSF	yes
2.1.1	2.1+2.0.1	2001	PSF	yes
2.1.2	2.1.1	2002	PSF	yes
2.1.3	2.1.2	2002	PSF	yes
2.2 and above	2.1.1	2001-now	PSF	yes

Footnotes:

(1) GPL-compatible doesn't mean that we're distributing Python under
    the GPL. All Python licenses, unlike the GPL, let you distribute
    a modified version without making your changes open source. The
    GPL-compatible licenses make it possible to combine Python with
    other software that is released under the GPL; the others don't.

(2) According to Richard Stallman, 1.6.1 is not GPL-compatible,
    because its license has a choice of law clause. According to
    CNRI, however, Stallman's lawyer has told CNRI's lawyer that 1.6.1
    is "not incompatible" with the GPL.

Thanks to the many outside volunteers who have worked under Guido's
direction to make these releases possible.

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1.100 protobuf-java 2.5.0

1.101 tiny-xml 2.4.0

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/** @mainpage

<h1> TinyXML </h1>

TinyXML is a simple, small, C++ XML parser that can be easily
integrated into other programs.

<h2> What it does. </h2>

In brief, TinyXML parses an XML document, and builds from that a
Document Object Model (DOM) that can be read, modified, and saved.

XML stands for "eXtensible Markup Language." It allows you to create

your own document markups. Where HTML does a very good job of marking
documents for browsers, XML allows you to define any kind of document
markup, for example a document that describes a "to do" list for an
organizer application. XML is a very structured and convenient format.
All those random file formats created to store application data can
all be replaced with XML. One parser for everything.

The best place for the complete, correct, and quite frankly hard to
read spec is at
http://www.w3.org/TR/2004/REC-xml-20040204/. An intro to XML
(that I really like) can be found at
http://skew.org/xml/tutorial.

There are different ways to access and interact with XML data.
TinyXML uses a Document Object Model (DOM), meaning the XML data is parsed
into a C++ objects that can be browsed and manipulated, and then
written to disk or another output stream. You can also construct an XML document
from scratch with C++ objects and write this to disk or another output
stream.

TinyXML is designed to be easy and fast to learn. It is two headers
and four cpp files. Simply add these to your project and off you go.
There is an example file - xmltest.cpp - to get you started.

TinyXML is released under the ZLib license,
so you can use it in open source or commercial code. The details
of the license are at the top of every source file.

TinyXML attempts to be a flexible parser, but with truly correct and
compliant XML output. TinyXML should compile on any reasonably C++
compliant system. It does not rely on exceptions or RTTI. It can be
compiled with or without STL support. TinyXML fully supports
the UTF-8 encoding, and the first 64k character entities.

<h2> What it doesn't do. </h2>

TinyXML doesn't parse or use DTDs (Document Type Definitions) or XSLs
(eXtensible Stylesheet Language.) There are other parsers out there
(check out www.sourceforge.org, search for XML) that are much more fully
featured. But they are also much bigger, take longer to set up in
your project, have a higher learning curve, and often have a more
restrictive license. If you are working with browsers or have more
complete XML needs, TinyXML is not the parser for you.

The following DTD syntax will not parse at this time in TinyXML:

@verbatim

```
<!DOCTYPE Archiv [
 <!ELEMENT Comment (#PCDATA)>
]>
@endverbatim
```

because TinyXML sees this as a !DOCTYPE node with an illegally
embedded !ELEMENT node. This may be addressed in the future.

<h2> Tutorials. </h2>

For the impatient, here is a tutorial to get you going. A great way to get started,
but it is worth your time to read this (very short) manual completely.

- @subpage tutorial0

<h2> Code Status. </h2>

TinyXML is mature, tested code. It is very stable. If you find
bugs, please file a bug report on the sourceforge web site
(www.sourceforge.net/projects/tinyxml). We'll get them straightened
out as soon as possible.

There are some areas of improvement; please check sourceforge if you are
interested in working on TinyXML.

<h2> Related Projects </h2>

TinyXML projects you may find useful! (Descriptions provided by the projects.)

 TinyXPath (http://tinyxpath.sourceforge.net). TinyXPath is a small footprint
    XPath syntax decoder, written in C++.
 TinyXML++ (http://code.google.com/p/ticpp/). TinyXML++ is a completely new
    interface to TinyXML that uses MANY of the C++ strengths. Templates,
  exceptions, and much better error handling.

<h2> Features </h2>

<h3> Using STL </h3>

TinyXML can be compiled to use or not use STL. When using STL, TinyXML
uses the std::string class, and fully supports std::istream, std::ostream,
operator<<, and operator>>. Many API methods have both 'const char*' and
'const std::string&' forms.

When STL support is compiled out, no STL files are included whatsoever. All
the string classes are implemented by TinyXML itself. API methods

all use the 'const char*' form for input.

Use the compile time #define:

 TIXML_USE_STL

to compile one version or the other. This can be passed by the compiler,
or set as the first line of "tinyxml.h".

Note: If compiling the test code in Linux, setting the environment
variable TINYXML_USE_STL=YES/NO will control STL compilation. In the
Windows project file, STL and non STL targets are provided. In your project,
It's probably easiest to add the line "#define TIXML_USE_STL" as the first
line of tinyxml.h.

<h3> UTF-8 </h3>

TinyXML supports UTF-8 allowing to manipulate XML files in any language. TinyXML
also supports "legacy mode" - the encoding used before UTF-8 support and
probably best described as "extended ascii".

Normally, TinyXML will try to detect the correct encoding and use it. However,
by setting the value of TIXML_DEFAULT_ENCODING in the header file, TinyXML
can be forced to always use one encoding.

TinyXML will assume Legacy Mode until one of the following occurs:

  If the non-standard but common "UTF-8 lead bytes" (0xef 0xbb 0xbf)
   begin the file or data stream, TinyXML will read it as UTF-8.
  If the declaration tag is read, and it has an encoding="UTF-8", then
   TinyXML will read it as UTF-8.
  If the declaration tag is read, and it has no encoding specified, then TinyXML will
   read it as UTF-8.
  If the declaration tag is read, and it has an encoding="something else", then TinyXML
   will read it as Legacy Mode. In legacy mode, TinyXML will work as it did before. It's
   not clear what that mode does exactly, but old content should keep working.
  Until one of the above criteria is met, TinyXML runs in Legacy Mode.

What happens if the encoding is incorrectly set or detected? TinyXML will try
to read and pass through text seen as improperly encoded. You may get some strange results or
mangled characters. You may want to force TinyXML to the correct mode.

You may force TinyXML to Legacy Mode by using LoadFile(TIXML_ENCODING_LEGACY) or
LoadFile(filename, TIXML_ENCODING_LEGACY). You may force it to use legacy mode all
the time by setting TIXML_DEFAULT_ENCODING = TIXML_ENCODING_LEGACY. Likewise, you may
force it to TIXML_ENCODING_UTF8 with the same technique.

For English users, using English XML, UTF-8 is the same as low-ASCII. You
don't need to be aware of UTF-8 or change your code in any way. You can think
of UTF-8 as a "superset" of ASCII.

UTF-8 is not a double byte format - but it is a standard encoding of Unicode!
TinyXML does not use or directly support wchar, TCHAR, or Microsoft's _UNICODE at this time.
It is common to see the term "Unicode" improperly refer to UTF-16, a wide byte encoding
of unicode. This is a source of confusion.

For "high-ascii" languages - everything not English, pretty much - TinyXML can
handle all languages, at the same time, as long as the XML is encoded
in UTF-8. That can be a little tricky, older programs and operating systems
tend to use the "default" or "traditional" code page. Many apps (and almost all
modern ones) can output UTF-8, but older or stubborn (or just broken) ones
still output text in the default code page.

For example, Japanese systems traditionally use SHIFT-JIS encoding.
Text encoded as SHIFT-JIS can not be read by TinyXML.
A good text editor can import SHIFT-JIS and then save as UTF-8.

The Skew.org link does a great
job covering the encoding issue.

The test file "utf8test.xml" is an XML containing English, Spanish, Russian,
and Simplified Chinese. (Hopefully they are translated correctly). The file
"utf8test.gif" is a screen capture of the XML file, rendered in IE. Note that
if you don't have the correct fonts (Simplified Chinese or Russian) on your
system, you won't see output that matches the GIF file even if you can parse
it correctly. Also note that (at least on my Windows machine) console output
is in a Western code page, so that Print() or printf() cannot correctly display
the file. This is not a bug in TinyXML - just an OS issue. No data is lost or
destroyed by TinyXML. The console just doesn't render UTF-8.

<h3> Entities </h3>
TinyXML recognizes the pre-defined "character entities", meaning special
characters. Namely:

@verbatim
& &
< <
> >
" "
' '
@endverbatim

These are recognized when the XML document is read, and translated to there
UTF-8 equivalents. For instance, text with the XML of:

@verbatim
 Far & Away
@endverbatim

will have the Value() of "Far & Away" when queried from the TiXmlText object,
and will be written back to the XML stream/file as an ampersand. Older versions
of TinyXML "preserved" character entities, but the newer versions will translate
them into characters.

Additionally, any character can be specified by its Unicode code point:
The syntax " " or " " are both to the non-breaking space characher.

<h3> Printing </h3>
TinyXML can print output in several different ways that all have strengths and limitations.

- Print(FILE*). Output to a std-C stream, which includes all C files as well as stdout.
 - "Pretty prints", but you don't have control over printing options.
 - The output is streamed directly to the FILE object, so there is no memory overhead
   in the TinyXML code.
 - used by Print() and SaveFile()

- operator<<. Output to a c++ stream.
 - Integrates with standart C++ iostreams.
 - Outputs in "network printing" mode without line breaks. Good for network transmission
   and moving XML between C++ objects, but hard for a human to read.

- TiXmlPrinter. Output to a std::string or memory buffer.
 - API is less concise
 - Future printing options will be put here.
 - Printing may change slightly in future versions as it is refined and expanded.

<h3> Streams </h3>
With TIXML_USE_STL on TinyXML supports C++ streams (operator <<,>>) streams as well
as C (FILE*) streams. There are some differences that you may need to be aware of.

C style output:
 - based on FILE*
 - the Print() and SaveFile() methods

 Generates formatted output, with plenty of white space, intended to be as
 human-readable as possible. They are very fast, and tolerant of ill formed
 XML documents. For example, an XML document that contains 2 root elements
 and 2 declarations, will still print.

C style input:
 - based on FILE*
 - the Parse() and LoadFile() methods

A fast, tolerant read. Use whenever you don't need the C++ streams.

C++ style output:
- based on std::ostream
- operator<<

Generates condensed output, intended for network transmission rather than
readability. Depending on your system's implementation of the ostream class,
these may be somewhat slower. (Or may not.) Not tolerant of ill formed XML:
a document should contain the correct one root element. Additional root level
elements will not be streamed out.

C++ style input:
- based on std::istream
- operator>>

Reads XML from a stream, making it useful for network transmission. The tricky
part is knowing when the XML document is complete, since there will almost
certainly be other data in the stream. TinyXML will assume the XML data is
complete after it reads the root element. Put another way, documents that
are ill-constructed with more than one root element will not read correctly.
Also note that operator>> is somewhat slower than Parse, due to both
implementation of the STL and limitations of TinyXML.

<h3> White space </h3>
The world simply does not agree on whether white space should be kept, or condensed.
For example, pretend the '_' is a space, and look at "Hello____world". HTML, and
at least some XML parsers, will interpret this as "Hello_world". They condense white
space. Some XML parsers do not, and will leave it as "Hello____world". (Remember
to keep pretending the _ is a space.) Others suggest that __Hello___world__ should become
Hello___world.

It's an issue that hasn't been resolved to my satisfaction. TinyXML supports the
first 2 approaches. Call TiXmlBase::SetCondenseWhiteSpace(bool) to set the desired behavior.
The default is to condense white space.

If you change the default, you should call TiXmlBase::SetCondenseWhiteSpace(bool)
before making any calls to Parse XML data, and I don't recommend changing it after
it has been set.

<h3> Handles </h3>

Where browsing an XML document in a robust way, it is important to check
for null returns from method calls. An error safe implementation can
generate a lot of code like:

```
@verbatim
TiXmlElement* root = document.FirstChildElement( "Document" );
if ( root )
{
 TiXmlElement* element = root->FirstChildElement( "Element" );
 if ( element )
 {
 TiXmlElement* child = element->FirstChildElement( "Child" );
 if ( child )
 {
  TiXmlElement* child2 = child->NextSiblingElement( "Child" );
  if ( child2 )
  {
   // Finally do something useful.
@endverbatim
```

Handles have been introduced to clean this up. Using the TiXmlHandle class,
the previous code reduces to:

```
@verbatim
TiXmlHandle docHandle( &document );
TiXmlElement* child2 = docHandle.FirstChild( "Document" ).FirstChild( "Element" ).Child( "Child", 1
).ToElement();
if ( child2 )
{
 // do something useful
@endverbatim
```

Which is much easier to deal with. See TiXmlHandle for more information.

<h3> Row and Column tracking </h3>
Being able to track nodes and attributes back to their origin location
in source files can be very important for some applications. Additionally,
knowing where parsing errors occured in the original source can be very
time saving.

TinyXML can tracks the row and column origin of all nodes and attributes
in a text file. The TiXmlBase::Row() and TiXmlBase::Column() methods return
the origin of the node in the source text. The correct tabs can be
configured in TiXmlDocument::SetTabSize().

<h2> Using and Installing </h2>

To Compile and Run xmltest:

A Linux Makefile and a Windows Visual C++ .dsw file is provided.

Simply compile and run. It will write the file demotest.xml to your
disk and generate output on the screen. It also tests walking the
DOM by printing out the number of nodes found using different
techniques.

The Linux makefile is very generic and runs on many systems - it
is currently tested on mingw and
MacOSX. You do not need to run 'make depend'. The dependecies have been
hard coded.

<h3>Windows project file for VC6</h3>

tinyxml: tinyxml library, non-STL
tinyxmlSTL: tinyxml library, STL
tinyXmlTest: test app, non-STL
tinyXmlTestSTL: test app, STL

<h3>Makefile</h3>
At the top of the makefile you can set:

PROFILE, DEBUG, and TINYXML_USE_STL. Details (such that they are) are in
the makefile.

In the tinyxml directory, type "make clean" then "make". The executable
file 'xmltest' will be created.

<h3>To Use in an Application:</h3>

Add tinyxml.cpp, tinyxml.h, tinyxmlerror.cpp, tinyxmlparser.cpp, tinystr.cpp, and tinystr.h to your
project or make file. That's it! It should compile on any reasonably
compliant C++ system. You do not need to enable exceptions or
RTTI for TinyXML.

<h2> How TinyXML works. </h2>

An example is probably the best way to go. Take:
@verbatim
 <?xml version="1.0" standalone=no>
 <!-- Our to do list data -->
 <ToDo>
  <Item priority="1"> Go to the <bold>Toy store!</bold></Item>
  <Item priority="2"> Do bills</Item>
 </ToDo>
@endverbatim

Its not much of a To Do list, but it will do. To read this file
(say "demo.xml") you would create a document, and parse it in:
@verbatim
 TiXmlDocument doc("demo.xml");
 doc.LoadFile();
@endverbatim

And its ready to go. Now lets look at some lines and how they
relate to the DOM.

@verbatim
<?xml version="1.0" standalone=no>
@endverbatim

The first line is a declaration, and gets turned into the
TiXmlDeclaration class. It will be the first child of the
document node.

This is the only directive/special tag parsed by TinyXML.
Generally directive tags are stored in TiXmlUnknown so the
commands wont be lost when it is saved back to disk.

@verbatim
<!-- Our to do list data -->
@endverbatim

A comment. Will become a TiXmlComment object.

@verbatim
<ToDo>
@endverbatim

The "ToDo" tag defines a TiXmlElement object. This one does not have
any attributes, but does contain 2 other elements.

@verbatim
<Item priority="1">
@endverbatim

Creates another TiXmlElement which is a child of the "ToDo" element.
This element has 1 attribute, with the name "priority" and the value
"1".

@verbatim
Go to the
@endverbatim

A TiXmlText. This is a leaf node and cannot contain other nodes.
It is a child of the "Item" TiXmlElement.

@verbatim
<bold>
@endverbatim

Another TiXmlElement, this one a child of the "Item" element.

Etc.

Looking at the entire object tree, you end up with:
@verbatim
TiXmlDocument   "demo.xml"
 TiXmlDeclaration   "version='1.0'" "standalone=no"
 TiXmlComment   " Our to do list data"
 TiXmlElement   "ToDo"
  TiXmlElement   "Item" Attribtutes: priority = 1
   TiXmlText   "Go to the "
   TiXmlElement "bold"
    TiXmlText "Toy store!"
  TiXmlElement   "Item" Attributes: priority=2
   TiXmlText   "Do bills"
@endverbatim

<h2> Documentation </h2>

The documentation is build with Doxygen, using the 'dox'
configuration file.

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<h2> References </h2>

The World Wide Web Consortium is the definitive standard body for
XML, and their web pages contain huge amounts of information.

The definitive spec:
http://www.w3.org/TR/2004/REC-xml-20040204/

I also recommend "XML Pocket Reference" by Robert Eckstein and published by
OReilly...the book that got the whole thing started.

<h2> Contributors, Contacts, and a Brief History </h2>

Thanks very much to everyone who sends suggestions, bugs, ideas, and
encouragement. It all helps, and makes this project fun. A special thanks
to the contributors on the web pages that keep it lively.

So many people have sent in bugs and ideas, that rather than list here
we try to give credit due in the "changes.txt" file.

TinyXML was originally written by Lee Thomason. (Often the "I" still
in the documentation.) Lee reviews changes and releases new versions,
with the help of Yves Berquin, Andrew Ellerton, and the tinyXml community.

We appreciate your suggestions, and would love to know if you
use TinyXML. Hopefully you will enjoy it and find it useful.
Please post questions, comments, file bugs, or contact us at:

www.sourceforge.net/projects/tinyxml

Lee Thomason, Yves Berquin, Andrew Ellerton
*/

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1.102 free-type 2.9.1

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#
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#
include/freetype/internal/fthash.h
#
src/base/fthash.c
src/base/md5.c
src/base/md5.h
#
src/bdf/bdf.c
src/bdf/bdf.h
src/bdf/bdfdrivr.c
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src/bdf/bdferror.h
src/bdf/bdflib.c
src/bdf/module.mk
src/bdf/README
src/bdf/rules.mk
#
src/pcf/module.mk
src/pcf/pcf.c
src/pcf/pcf.h
src/pcf/pcfdrivr.c
src/pcf/pcfdrivr.h
src/pcf/pcferror.h
src/pcf/pcfread.c
src/pcf/pcfread.h
src/pcf/pcfutil.c
src/pcf/pcfutil.h
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src/pcf/rules.mk
#
src/gzip/adler32.c
src/gzip/infblock.c
src/gzip/infblock.h
src/gzip/infcodes.c
src/gzip/infcodes.h
src/gzip/inffixed.h
src/gzip/inflate.c
src/gzip/inftrees.c
src/gzip/inftrees.h
src/gzip/infutil.c

src/gzip/infutil.h
src/gzip/zconf.h
src/gzip/zlib.h
src/gzip/zutil.c
src/gzip/zutil.h
#
src/tools/apinames.c
src/tools/ftrandom/ftrandom.c
#
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1.103 gdisk 0.8.10

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jar/com/mastfrog/jackson/DurationSerializationMode.java
* /opt/ws_local/PERMITS_SQL/1078139564_1597259690.4/0/jackson-2-6-6-sources-1-
jar/com/mastfrog/jackson/LocaleJacksonConfigurer.java
* /opt/ws_local/PERMITS_SQL/1078139564_1597259690.4/0/jackson-2-6-6-sources-1-
jar/com/mastfrog/jackson/JavaTimeConfigurer.java
* /opt/ws_local/PERMITS_SQL/1078139564_1597259690.4/0/jackson-2-6-6-sources-1-
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No license file was found, but licenses were detected in source scan.

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* /opt/ws_local/PERMITS_SQL/1078139564_1597259690.4/0/jackson-2-6-6-sources-1-jar/com/mastfrog/jackson/OptionalSerializer.java

* /opt/ws_local/PERMITS_SQL/1078139564_1597259690.4/0/jackson-2-6-6-sources-1-jar/com/mastfrog/jackson/OptionalJavaUtilSerializer.java

1.109 libvpx v1.11.0

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1.110 libcxx 8.0.1

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; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=aarch64-- | FileCheck %s

; A shuffle mask with all undef elements is always legal.

```
define <4 x i32> @PR41535(<2 x i32> %p1, <2 x i32> %p2) {
; CHECK-LABEL: PR41535:
; CHECK:       // %bb.0:
; CHECK-NEXT:    ext v0.8b, v0.8b, v1.8b, #4
; CHECK-NEXT:    mov v0.d[1], v0.d[0]
; CHECK-NEXT:    ret
  %cat1 = shufflevector <2 x i32> %p1, <2 x i32> undef, <4 x i32> <i32 undef, i32 1, i32 undef, i32 undef>
  %cat2 = shufflevector <2 x i32> %p2, <2 x i32> undef, <4 x i32> <i32 0, i32 undef, i32 undef, i32 undef>
  %r = shufflevector <4 x i32> %cat1, <4 x i32> %cat2, <4 x i32> <i32 undef, i32 undef, i32 1, i32 4>
  ret <4 x i32> %r
}
```
; RUN: llc < %s -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
;
; Test that early if conversion produces LOCR with operands of the right
; register classes.

```
define void @autogen_SD4739(i8*) {
```

```
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
 %L34 = load i8, i8* %0
 %Cmp56 = icmp sgt i8 undef, %L34
 br label %CF246

CF246:                                ; preds = %CF246, %BB
 %Sl163 = select i1 %Cmp56, i8 %L34, i8 undef
 br i1 undef, label %CF246, label %CF248

CF248:                                ; preds = %CF248, %CF246
 store i8 %Sl163, i8* %0
 br label %CF248
}
```

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```
; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --check-attributes --check-globals
; RUN: opt -attributor -enable-new-pm=0 -attributor-manifest-internal  -attributor-max-iterations-verify -attributor-annotate-decl-cs -attributor-max-iterations=6 -S < %s | FileCheck %s --check-prefixes=CHECK,NOT_CGSCC_NPM,NOT_CGSCC_OPM,NOT_TUNIT_NPM,IS__TUNIT____,IS_____OPM,IS__TUNIT_OPM
; RUN: opt -aa-pipeline=basic-aa -passes=attributor -attributor-manifest-internal  -attributor-max-iterations-verify -attributor-annotate-decl-cs -attributor-max-iterations=6 -S < %s | FileCheck %s --check-prefixes=CHECK,NOT_CGSCC_OPM,NOT_CGSCC_NPM,NOT_TUNIT_OPM,IS__TUNIT____,IS_____NPM,IS__TUNIT_NPM
; RUN: opt -attributor-cgscc -enable-new-pm=0 -attributor-manifest-internal  -attributor-annotate-decl-cs -S < %s | FileCheck %s --check-prefixes=CHECK,NOT_TUNIT_NPM,NOT_TUNIT_OPM,NOT_CGSCC_NPM,IS__CGSCC____,IS_____OPM,IS__CGSCC_OPM
; RUN: opt -aa-pipeline=basic-aa -passes=attributor-cgscc -attributor-manifest-internal  -attributor-annotate-decl-cs -S < %s | FileCheck %s --check-prefixes=CHECK,NOT_TUNIT_NPM,NOT_TUNIT_OPM,NOT_CGSCC_OPM,IS__CGSCC____,IS_____NPM,IS__CGSCC_NPM
; Test that we only promote arguments when the caller/callee have compatible
; function attrubtes.

target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
```

```
#[[ATTR0:[0-9]+]] {
; IS_____OPM-NEXT:  bb:
; IS_____OPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT:    ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR0:[0-9]+]] {
; IS__TUNIT_NPM-NEXT:  bb:
; IS__TUNIT_NPM-NEXT:    [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT:    ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR0:[0-9]+]] {
; IS__CGSCC_NPM-NEXT:  bb:
; IS__CGSCC_NPM-NEXT:    [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT:    ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}


define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR0]] {
; IS__TUNIT_OPM-NEXT:  bb:
; IS__TUNIT_OPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6:[0-9]+]]
; IS__TUNIT_OPM-NEXT:    call fastcc void
```

@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7:[0-9]+]]

; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64

; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2

; IS__TUNIT_OPM-NEXT: ret void

;

; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn

; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512

; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR0]] {

; IS__TUNIT_NPM-NEXT: bb:

; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*

; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6:[0-9]+]]

; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64

; IS__TUNIT_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7:[0-9]+]]

; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64

; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2

; IS__TUNIT_NPM-NEXT: ret void

;

; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn

; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512

; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR0]] {

; IS__CGSCC_OPM-NEXT: bb:

; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*

; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6:[0-9]+]]

; IS__CGSCC_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7:[0-9]+]]

; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64

; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2

; IS__CGSCC_OPM-NEXT: ret void

;

; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn

; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512

; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR0]] {

; IS__CGSCC_NPM-NEXT: bb:

; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

```
; IS__CGSCC_NPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6:[0-9]+]]
; IS__CGSCC_NPM-NEXT:    [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_NPM-NEXT:    call fastcc void
@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7:[0-9]+]]
; IS__CGSCC_NPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:    ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}


; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR1:[0-9]+]] {
; IS_____OPM-NEXT:  bb:
; IS_____OPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT:    ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1:[0-9]+]] {
; IS__TUNIT_NPM-NEXT:  bb:
; IS__TUNIT_NPM-NEXT:    [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
```

; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1:[0-9]+]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP0]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly

align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]

; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64

; IS__TUNIT_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]

; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64

; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2

; IS__TUNIT_NPM-NEXT: ret void

;

; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn

; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256

; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR1]] {

; IS__CGSCC_OPM-NEXT: bb:

; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*

; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]

; IS__CGSCC_OPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]

; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64

; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2

; IS__CGSCC_OPM-NEXT: ret void

;

; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn

; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256

; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR1]] {

; IS__CGSCC_NPM-NEXT: bb:

; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32

; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*

; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]

; IS__CGSCC_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64

; IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]

; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64

; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2

; IS__CGSCC_NPM-NEXT: ret void

;

bb:

 %tmp = alloca <8 x i64>, align 32

 %tmp2 = alloca <8 x i64>, align 32

```
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}


; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR1]] {
; IS_____OPM-NEXT:  bb:
; IS_____OPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT:    ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1]] {
; IS__TUNIT_NPM-NEXT:  bb:
; IS__TUNIT_NPM-NEXT:    [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT:    ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR1]] {
; IS__CGSCC_NPM-NEXT:  bb:
; IS__CGSCC_NPM-NEXT:    [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT:    ret void
;
```

```
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}
```

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR0]] {
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR0]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR0]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32

; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR0]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define

```
{{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR0]] {
; IS_____OPM-NEXT: bb:
; IS_____OPM-NEXT:   [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT:   store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT:   ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR0]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT:   [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT:   store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:   [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:   store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT:   ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR0]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT:   [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT:   store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:   [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:   store <8 x i64> [[TMP0]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT:   ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT:   [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:   [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:   [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
```

; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR1]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)

[[ARG:%.*]]) #[[ATTR1]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_NPM-NEXT: call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT: ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define
{{[^@]+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR1]] {
; IS_____OPM-NEXT: bb:
; IS_____OPM-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT: ret void
;
; IS_____NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS_____NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree noundef nonnull readonly align 64
dereferenceable(64) [[ARG1:%.*]]) #[[ATTR1:[0-9]+]] {

```
; IS_____NPM-NEXT:  bb:
; IS_____NPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____NPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____NPM-NEXT:    ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}


define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR2:[0-9]+]] {
; IS__TUNIT_OPM-NEXT:  bb:
; IS__TUNIT_OPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT:    call fastcc void
@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT:    ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR2:[0-9]+]] {
; IS__TUNIT_NPM-NEXT:  bb:
; IS__TUNIT_NPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT:    call fastcc void
@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree noundef
nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT:    ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
```

```
; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR2:[0-9]+]] {
; IS__CGSCC_OPM-NEXT:  bb:
; IS__CGSCC_OPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT:    call fastcc void
@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* nocapture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT:    ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR2:[0-9]+]] {
; IS__CGSCC_NPM-NEXT:  bb:
; IS__CGSCC_NPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT:    call fastcc void
@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree noundef
nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:    ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}

; This should not promote
```

```
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #2 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR2:[0-9]+]] {
; IS_____OPM-NEXT:  bb:
; IS_____OPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT:    ret void
;
; IS_____NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____NPM-LABEL: define
{{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS_____NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64>* noalias nocapture nofree noundef nonnull readonly align 64
dereferenceable(64) [[ARG1:%.*]]) #[[ATTR2:[0-9]+]] {
; IS_____NPM-NEXT:  bb:
; IS_____NPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____NPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____NPM-NEXT:    ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT_OPM-NEXT:  bb:
; IS__TUNIT_OPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT:    call fastcc void
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* nocapture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly
align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
```

; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR1]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR1]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR1]] {
; IS__CGSCC_NPM-NEXT: bb:
; IS__CGSCC_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT: call fastcc void

```
@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* noalias nocapture nofree
noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* noalias nocapture nofree noundef
nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:    ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}


; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8
x i64>* readonly %arg1) #3 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define {{[^@]+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR3:[0-9]+]] {
; IS_____OPM-NEXT:  bb:
; IS_____OPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT:    ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR3:[0-9]+]] {
; IS__TUNIT_NPM-NEXT:  bb:
; IS__TUNIT_NPM-NEXT:    [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT:    ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR3:[0-9]+]] {
```

```
; IS__CGSCC_NPM-NEXT:  bb:
; IS__CGSCC_NPM-NEXT:    [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT:    ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}


define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR4:[0-9]+]] {
; IS__TUNIT_OPM-NEXT:  bb:
; IS__TUNIT_OPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT:    call fastcc void
@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* nocapture nofree noundef nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64
dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT:    ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR4:[0-9]+]] {
; IS__TUNIT_NPM-NEXT:  bb:
; IS__TUNIT_NPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT:    [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT:    call fastcc void
@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocapture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT:    ret void
```

```
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR4:[0-9]+]] {
; IS__CGSCC_OPM-NEXT:  bb:
; IS__CGSCC_OPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT:    call fastcc void
@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* nocapture nofree noundef nonnull
writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64
dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT:    ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR4:[0-9]+]] {
; IS__CGSCC_NPM-NEXT:  bb:
; IS__CGSCC_NPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT:    [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_NPM-NEXT:    call fastcc void
@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* noalias nocapture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:    ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}
```

```
; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8
x i64>* readonly %arg1) #4 {
;
; IS_____OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS_____OPM-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS_____OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64)
[[ARG:%.*]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[ARG1:%.*]])
#[[ATTR4:[0-9]+]] {
; IS_____OPM-NEXT:  bb:
; IS_____OPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]], align 64
; IS_____OPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS_____OPM-NEXT:    ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR4]] {
; IS__TUNIT_NPM-NEXT:  bb:
; IS__TUNIT_NPM-NEXT:    [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__TUNIT_NPM-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]], align 64
; IS__TUNIT_NPM-NEXT:    ret void
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64
dereferenceable(64) [[ARG:%.*]], <8 x i64> [[TMP0:%.*]]) #[[ATTR4]] {
; IS__CGSCC_NPM-NEXT:  bb:
; IS__CGSCC_NPM-NEXT:    [[ARG1_PRIV:%.*]] = alloca <8 x i64>, align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1_PRIV]], align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP0]], <8 x i64>* [[ARG]], align 64
; IS__CGSCC_NPM-NEXT:    ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}

define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
;
; IS__TUNIT_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_OPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__TUNIT_OPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR3]] {
```

; IS__TUNIT_OPM-NEXT: bb:
; IS__TUNIT_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_OPM-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__TUNIT_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_OPM-NEXT: ret void
;
; IS__TUNIT_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__TUNIT_NPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__TUNIT_NPM-SAME: (<8 x i64>* nocapture nofree writeonly [[ARG:%.*]]) #[[ATTR3]] {
; IS__TUNIT_NPM-NEXT: bb:
; IS__TUNIT_NPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__TUNIT_NPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__TUNIT_NPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__TUNIT_NPM-NEXT: [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__TUNIT_NPM-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__TUNIT_NPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__TUNIT_NPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__TUNIT_NPM-NEXT: ret void
;
; IS__CGSCC_OPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_OPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__CGSCC_OPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64) [[ARG:%.*]]) #[[ATTR3]] {
; IS__CGSCC_OPM-NEXT: bb:
; IS__CGSCC_OPM-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_OPM-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_OPM-NEXT: call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_OPM-NEXT: call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* nocapture nofree noundef nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64>* nocapture nofree noundef nonnull readonly align 64 dereferenceable(64) [[TMP]]) #[[ATTR7]]
; IS__CGSCC_OPM-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_OPM-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_OPM-NEXT: ret void

```
;
; IS__CGSCC_NPM: Function Attrs: argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn
; IS__CGSCC_NPM-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; IS__CGSCC_NPM-SAME: (<8 x i64>* nocapture nofree noundef nonnull writeonly align 2 dereferenceable(64)
[[ARG:%.*]]) #[[ATTR3]] {
; IS__CGSCC_NPM-NEXT:  bb:
; IS__CGSCC_NPM-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; IS__CGSCC_NPM-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; IS__CGSCC_NPM-NEXT:    call void @llvm.memset.p0i8.i64(i8* nocapture nofree noundef nonnull writeonly
align 64 dereferenceable(64) [[TMP3]], i8 noundef 0, i64 noundef 32, i1 noundef false) #[[ATTR6]]
; IS__CGSCC_NPM-NEXT:    [[TMP0:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]], align 64
; IS__CGSCC_NPM-NEXT:    call fastcc void
@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* noalias nocapture nofree noundef
nonnull writeonly align 64 dereferenceable(64) [[TMP2]], <8 x i64> [[TMP0]]) #[[ATTR7]]
; IS__CGSCC_NPM-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 64
; IS__CGSCC_NPM-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; IS__CGSCC_NPM-NEXT:    ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}

; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5

attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512"
"prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256"
"prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }
;.
; IS__TUNIT____: attributes #[[ATTR0:[0-9]+]] = { argmemonly inlinehint nofree norecurse nosync nounwind
uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="512" "target-features"="+avx512vl" }
```

; IS__TUNIT____: attributes #[[ATTR1:[0-9]+]] = { argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx512vl" }
; IS__TUNIT____: attributes #[[ATTR2:[0-9]+]] = { argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn "min-legal-vector-width"="256" "prefer-vector-width"="256" "target-features"="+avx512vl" }
; IS__TUNIT____: attributes #[[ATTR3:[0-9]+]] = { argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx2" }
; IS__TUNIT____: attributes #[[ATTR4:[0-9]+]] = { argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn "min-legal-vector-width"="256" "prefer-vector-width"="256" "target-features"="+avx2" }
; IS__TUNIT____: attributes #[[ATTR5:[0-9]+]] = { argmemonly nofree nounwind willreturn writeonly }
; IS__TUNIT____: attributes #[[ATTR6:[0-9]+]] = { willreturn writeonly }
; IS__TUNIT____: attributes #[[ATTR7:[0-9]+]] = { nofree nosync nounwind willreturn }
;.
; IS__CGSCC____: attributes #[[ATTR0:[0-9]+]] = { argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="512" "target-features"="+avx512vl" }
; IS__CGSCC____: attributes #[[ATTR1:[0-9]+]] = { argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx512vl" }
; IS__CGSCC____: attributes #[[ATTR2:[0-9]+]] = { argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn "min-legal-vector-width"="256" "prefer-vector-width"="256" "target-features"="+avx512vl" }
; IS__CGSCC____: attributes #[[ATTR3:[0-9]+]] = { argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn "min-legal-vector-width"="512" "prefer-vector-width"="256" "target-features"="+avx2" }
; IS__CGSCC____: attributes #[[ATTR4:[0-9]+]] = { argmemonly inlinehint nofree norecurse nosync nounwind uwtable willreturn "min-legal-vector-width"="256" "prefer-vector-width"="256" "target-features"="+avx2" }
; IS__CGSCC____: attributes #[[ATTR5:[0-9]+]] = { argmemonly nofree nounwind willreturn writeonly }
; IS__CGSCC____: attributes #[[ATTR6:[0-9]+]] = { willreturn writeonly }
; IS__CGSCC____: attributes #[[ATTR7:[0-9]+]] = { nounwind willreturn }
;.
; RUN: opt -mtriple=aarch64-linux-gnu -mattr=+sve -scalarize-masked-mem-intrin -S < %s | FileCheck %s

; Testing that masked gathers operating on scalable vectors that are
; packed in SVE registers are not scalarized.

; CHECK-LABEL: @masked_gather_nxv4i32(
; CHECK: call <vscale x 4 x i32> @llvm.masked.gather.nxv4i32
define <vscale x 4 x i32> @masked_gather_nxv4i32(<vscale x 4 x i32*> %ld, <vscale x 4 x i1> %masks, <vscale x 4 x i32> %passthru) {
 %res = call <vscale x 4 x i32> @llvm.masked.gather.nxv4i32(<vscale x 4 x i32*> %ld, i32 0, <vscale x 4 x i1> %masks, <vscale x 4 x i32> %passthru)
 ret <vscale x 4 x i32> %res
}

; Testing that masked gathers operating on scalable vectors of FP data
; that is packed in SVE registers are not scalarized.

; CHECK-LABEL: @masked_gather_nxv2f64(
; CHECK: call <vscale x 2 x double> @llvm.masked.gather.nxv2f64
define <vscale x 2 x double> @masked_gather_nxv2f64(<vscale x 2 x double*> %ld, <vscale x 2 x i1> %masks, <vscale x 2 x double> %passthru) {
 %res = call <vscale x 2 x double> @llvm.masked.gather.nxv2f64(<vscale x 2 x double*> %ld, i32 0, <vscale x 2 x

```
i1> %masks, <vscale x 2 x double> %passthru)
 ret <vscale x 2 x double> %res
}


; Testing that masked gathers operating on scalable vectors of FP data
; that is unpacked in SVE registers are not scalarized.

; CHECK-LABEL: @masked_gather_nxv2f16(
; CHECK: call <vscale x 2 x half> @llvm.masked.gather.nxv2f16
define <vscale x 2 x half> @masked_gather_nxv2f16(<vscale x 2 x half*> %ld, <vscale x 2 x i1> %masks, <vscale
x 2 x half> %passthru) {
 %res = call <vscale x 2 x half> @llvm.masked.gather.nxv2f16(<vscale x 2 x half*> %ld, i32 0, <vscale x 2 x i1>
%masks, <vscale x 2 x half> %passthru)
 ret <vscale x 2 x half> %res
}


; Testing that masked gathers operating on 64-bit fixed vectors are
; scalarized because NEON doesn't have support for masked gather
; instructions.

; CHECK-LABEL: @masked_gather_v2f32(
; CHECK-NOT: @llvm.masked.gather.v2f32(
define <2 x float> @masked_gather_v2f32(<2 x float*> %ld, <2 x i1> %masks, <2 x float> %passthru) {
 %res = call <2 x float> @llvm.masked.gather.v2f32(<2 x float*> %ld, i32 0, <2 x i1> %masks, <2 x float>
%passthru)
 ret <2 x float> %res
}


; Testing that masked gathers operating on 128-bit fixed vectors are
; scalarized because NEON doesn't have support for masked gather
; instructions and because we are not targeting fixed width SVE.

; CHECK-LABEL: @masked_gather_v4i32(
; CHECK-NOT: @llvm.masked.gather.v4i32(
define <4 x i32> @masked_gather_v4i32(<4 x i32*> %ld, <4 x i1> %masks, <4 x i32> %passthru) {
 %res = call <4 x i32> @llvm.masked.gather.v4i32(<4 x i32*> %ld, i32 0, <4 x i1> %masks, <4 x i32> %passthru)
 ret <4 x i32> %res
}

declare <vscale x 4 x i32> @llvm.masked.gather.nxv4i32(<vscale x 4 x i32*> %ptrs, i32 %align, <vscale x 4 x i1>
%masks, <vscale x 4 x i32> %passthru)
declare <vscale x 2 x double> @llvm.masked.gather.nxv2f64(<vscale x 2 x double*> %ptrs, i32 %align, <vscale x
2 x i1> %masks, <vscale x 2 x double> %passthru)
declare <vscale x 2 x half> @llvm.masked.gather.nxv2f16(<vscale x 2 x half*> %ptrs, i32 %align, <vscale x 2 x
i1> %masks, <vscale x 2 x half> %passthru)
declare <2 x float> @llvm.masked.gather.v2f32(<2 x float*> %ptrs, i32 %align, <2 x i1> %masks, <2 x float>
%passthru)
declare <4 x i32> @llvm.masked.gather.v4i32(<4 x i32*> %ptrs, i32 %align, <4 x i1> %masks, <4 x i32>
```

%passthru)
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```
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s
;
; D31946
; Check that we dont end up with the ""LLVM ERROR: Cannot select" error.
; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128, fp128)

define fp128 @TestSelect(fp128 %a, fp128 %b) {
; CHECK-LABEL: TestSelect:
; CHECK:       # %bb.0:
; CHECK-NEXT:    pushq %rbx
; CHECK-NEXT:    .cfi_def_cfa_offset 16
; CHECK-NEXT:    subq $32, %rsp
; CHECK-NEXT:    .cfi_def_cfa_offset 48
; CHECK-NEXT:    .cfi_offset %rbx, -16
; CHECK-NEXT:    movaps %xmm1, {{[-0-9]+}}(%r{{[sb]}}p) # 16-byte Spill
; CHECK-NEXT:    movaps %xmm0, (%rsp) # 16-byte Spill
; CHECK-NEXT:    callq __gttf2@PLT
; CHECK-NEXT:    movl %eax, %ebx
; CHECK-NEXT:    movaps (%rsp), %xmm0 # 16-byte Reload
; CHECK-NEXT:    movaps {{[-0-9]+}}(%r{{[sb]}}p), %xmm1 # 16-byte Reload
; CHECK-NEXT:    callq __subtf3@PLT
; CHECK-NEXT:    testl %ebx, %ebx
; CHECK-NEXT:    jg .LBB0_2
; CHECK-NEXT:  # %bb.1:
; CHECK-NEXT:    xorps %xmm0, %xmm0
; CHECK-NEXT:  .LBB0_2:
; CHECK-NEXT:    addq $32, %rsp
; CHECK-NEXT:    .cfi_def_cfa_offset 16
; CHECK-NEXT:    popq %rbx
; CHECK-NEXT:    .cfi_def_cfa_offset 8
; CHECK-NEXT:    retq
  %cmp = fcmp ogt fp128 %a, %b
  %sub = fsub fp128 %a, %b
```

```
%res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000
 ret fp128 %res
}

define fp128 @TestFabs(fp128 %a) {
; CHECK-LABEL: TestFabs:
; CHECK:       # %bb.0:
; CHECK-NEXT:    andps {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm0
; CHECK-NEXT:    retq
 %res = call fp128 @llvm.fabs.f128(fp128 %a)
 ret fp128 %res
}

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
; CHECK-LABEL: TestCopysign:
; CHECK:       # %bb.0:
; CHECK-NEXT:    andps {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm1
; CHECK-NEXT:    andps {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm0
; CHECK-NEXT:    orps %xmm1, %xmm0
; CHECK-NEXT:    retq
 %res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
 ret fp128 %res
}

define fp128 @TestFneg(fp128 %a) {
; CHECK-LABEL: TestFneg:
; CHECK:       # %bb.0:
; CHECK-NEXT:    pushq %rax
; CHECK-NEXT:    .cfi_def_cfa_offset 16
; CHECK-NEXT:    movaps %xmm0, %xmm1
; CHECK-NEXT:    callq __multf3@PLT
; CHECK-NEXT:    xorps {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm0
; CHECK-NEXT:    popq %rax
; CHECK-NEXT:    .cfi_def_cfa_offset 8
; CHECK-NEXT:    retq
 %mul = fmul fp128 %a, %a
 %res = fsub fp128 0xL00000000000000008000000000000000, %mul
 ret fp128 %res
}
```

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```
; RUN: opt %s -inline -S | FileCheck %s

define internal void @innerSmall() "min-legal-vector-width"="128" {
 ret void
}

define internal void @innerLarge() "min-legal-vector-width"="512" {
 ret void
}

define internal void @innerNoAttribute() {
 ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.
define void @outerNoAttribute() {
 call void @innerLarge()
 ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
 call void @innerLarge()
 ret void
}

define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
 call void @innerSmall()
 ret void
}

; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
 call void @innerNoAttribute()
 ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }
; RUN: opt -consthoist -S -o - %s | FileCheck %s
target datalayout = "e-m:e-p:32:32-i64:64-v128:64:128-a:0:32-n32-S64"
```

target triple = "thumbv6m-none--musleabi"

; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
; CHECK: foo_i8
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874720 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK-DAG: %[[C3:const[0-9]?]] = bitcast i32 805873720 to i32
; CHECK-DAG: %[[C4:const[0-9]?]] = bitcast i32 805873688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i8*
; CHECK-NEXT: %1 = load volatile i8, i8* %0
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i8*
; CHECK-NEXT: %3 = load volatile i8, i8* %2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 31
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i8*
; CHECK-NEXT: %5 = load volatile i8, i8* %4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i8*
; CHECK-NEXT: %7 = load volatile i8, i8* %6
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 7
; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i8*
; CHECK-NEXT: %9 = load volatile i8, i8* %8
; CHECK-NEXT: %10 = inttoptr i32 %[[C4]] to i8*
; CHECK-NEXT: store i8 %9, i8* %10
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C4]], 31
; CHECK-NEXT: %11 = inttoptr i32 %[[M4]] to i8*
; CHECK-NEXT: store i8 %7, i8* %11
; CHECK-NEXT: %12 = inttoptr i32 %[[C3]] to i8*
; CHECK-NEXT: store i8 %5, i8* %12
; CHECK-NEXT: %[[M5:const_mat[0-9]?]] = add i32 %[[C3]], 7
; CHECK-NEXT: %13 = inttoptr i32 %[[M5]] to i8*
; CHECK-NEXT: store i8 %3, i8* %13
; CHECK-NEXT: %[[M6:const_mat[0-9]?]] = add i32 %[[C1]], 80
; CHECK-NEXT: %14 = inttoptr i32 %[[M6]] to i8*
; CHECK-NEXT: store i8* %14, i8** @goo

@goo = global i8* undef

define void @foo_i8() {
entry:
 %0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
 %1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
 %2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
 %3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
 %4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
 store i8 %4, i8* inttoptr(i32 805873688 to i8*)
 store i8 %3, i8* inttoptr(i32 805873719 to i8*)

```
  store i8 %2, i8* inttoptr(i32 805873720 to i8*)
  store i8 %1, i8* inttoptr(i32 805873727 to i8*)
  store i8* inttoptr(i32 805874800 to i8*), i8** @goo
  ret void
}
```

; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 22
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %11 = load volatile i16, i16* %10, align 2

define void @foo_i16() {
entry:
 %0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
 %1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
 %2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
 %3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
 %4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
 %5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
 ret void
}

; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i32*
; CHECK-NEXT: %3 = load volatile i32, i32* %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 124
```

```
; CHECK-NEXT:  %4 = inttoptr i32 %[[M2]] to i32*
; CHECK-NEXT:  %5 = load volatile i32, i32* %4, align 4
; CHECK-NEXT:  %6 = inttoptr i32 %[[C1]] to i32*
; CHECK-NEXT:  %7 = load volatile i32, i32* %6, align 4
; CHECK-NEXT:  %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 8
; CHECK-NEXT:  %8 = inttoptr i32 %[[M3]] to i32*
; CHECK-NEXT:  %9 = load volatile i32, i32* %8, align 4
; CHECK-NEXT:  %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 12
; CHECK-NEXT:  %10 = inttoptr i32 %[[M4]] to i32*
; CHECK-NEXT:  %11 = load volatile i32, i32* %10, align 4

define void @foo_i32() {
entry:
 %0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
 %1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
 %2 = load volatile i32, i32* inttoptr (i32 805874812 to i32*), align 4
 %3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
 %4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
 %5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
 ret void
}
```

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----
clang-tidy CERT Files

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de Minimis description of such content.
; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --function-signature --
scrub-attributes
; RUN: opt -S -argpromotion < %s | FileCheck %s
; RUN: opt -S -passes=argpromotion < %s | FileCheck %s

; Test that we only promote arguments when the caller/callee have compatible
; function attrubtes.

target triple = "x86_64-unknown-linux-gnu"

; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #0 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}

define void @avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %arg) #0 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x
i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}

; This should promote

```
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:    store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT:    ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}


define void @avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:    call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:    [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT:    call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x
i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:    ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}


; This should promote
define internal fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:    store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
```

```
; CHECK-NEXT:    ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}


define void @avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %arg) #0 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer512_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:    call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:    [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT:    call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:    ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx512_legal512_prefer512_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}


; This should promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #0 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:    store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT:    ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
```

```
}

define void @avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal512_prefer512
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:    call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:    [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT:    call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x
i64>* [[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:    ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal512_prefer512(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}


; This should not promote
define internal fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg,
<8 x i64>* readonly %arg1) #1 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:    [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
; CHECK-NEXT:    store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
; CHECK-NEXT:    ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}

define void @avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %arg) #2 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
```

; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* [[TMP2]], <8 x i64>* [[TMP]])
; CHECK-NEXT: [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT: store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT: ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>* %tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}

; This should not promote
define internal fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg, <8 x i64>* readonly %arg1) #2 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64>* readonly [[ARG1:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = load <8 x i64>, <8 x i64>* [[ARG1]]
; CHECK-NEXT: store <8 x i64> [[TMP]], <8 x i64>* [[ARG]]
; CHECK-NEXT: ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}

define void @avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %arg) #1 {
; CHECK-LABEL: define {{[^@]+}}@avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT: bb:
; CHECK-NEXT: [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT: [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT: call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT: call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x

```
i64>* [[TMP2]], <8 x i64>* [[TMP]])
; CHECK-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:    ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(<8 x i64>* %tmp2, <8 x
i64>* %tmp)
 %tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
 store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
 ret void
}


; This should promote
define internal fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg, <8
x i64>* readonly %arg1) #3 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:    store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT:    ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}


define void @avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %arg) #4 {
; CHECK-LABEL: define {{[^@]+}}@avx2_legal256_prefer256_call_avx2_legal512_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:    call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:    [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT:    call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>*
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:    ret void
;
bb:
```

```
%tmp = alloca <8 x i64>, align 32
%tmp2 = alloca <8 x i64>, align 32
%tmp3 = bitcast <8 x i64>* %tmp to i8*
call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
call fastcc void @callee_avx2_legal256_prefer256_call_avx2_legal512_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}


; This should promote
define internal fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg, <8
x i64>* readonly %arg1) #4 {
; CHECK-LABEL: define {{[^@]+}}@callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]], <8 x i64> [[ARG1_VAL:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:    store <8 x i64> [[ARG1_VAL]], <8 x i64>* [[ARG]]
; CHECK-NEXT:    ret void
;
bb:
 %tmp = load <8 x i64>, <8 x i64>* %arg1
 store <8 x i64> %tmp, <8 x i64>* %arg
 ret void
}


define void @avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %arg) #3 {
; CHECK-LABEL: define {{[^@]+}}@avx2_legal512_prefer256_call_avx2_legal256_prefer256
; CHECK-SAME: (<8 x i64>* [[ARG:%.*]])
; CHECK-NEXT:  bb:
; CHECK-NEXT:    [[TMP:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:    [[TMP2:%.*]] = alloca <8 x i64>, align 32
; CHECK-NEXT:    [[TMP3:%.*]] = bitcast <8 x i64>* [[TMP]] to i8*
; CHECK-NEXT:    call void @llvm.memset.p0i8.i64(i8* align 32 [[TMP3]], i8 0, i64 32, i1 false)
; CHECK-NEXT:    [[TMP_VAL:%.*]] = load <8 x i64>, <8 x i64>* [[TMP]]
; CHECK-NEXT:    call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>*
[[TMP2]], <8 x i64> [[TMP_VAL]])
; CHECK-NEXT:    [[TMP4:%.*]] = load <8 x i64>, <8 x i64>* [[TMP2]], align 32
; CHECK-NEXT:    store <8 x i64> [[TMP4]], <8 x i64>* [[ARG]], align 2
; CHECK-NEXT:    ret void
;
bb:
 %tmp = alloca <8 x i64>, align 32
 %tmp2 = alloca <8 x i64>, align 32
 %tmp3 = bitcast <8 x i64>* %tmp to i8*
 call void @llvm.memset.p0i8.i64(i8* align 32 %tmp3, i8 0, i64 32, i1 false)
 call fastcc void @callee_avx2_legal512_prefer256_call_avx2_legal256_prefer256(<8 x i64>* %tmp2, <8 x i64>*
%tmp)
```

```
%tmp4 = load <8 x i64>, <8 x i64>* %tmp2, align 32
store <8 x i64> %tmp4, <8 x i64>* %arg, align 2
ret void
}


; If the arguments are scalar, its ok to promote.
define internal i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %X, i32*
%Y) #2 {
; CHECK-LABEL: define
{{[^@]+}}@scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (i32 [[X_VAL:%.*]], i32 [[Y_VAL:%.*]])
; CHECK-NEXT:    [[C:%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
; CHECK-NEXT:    ret i32 [[C]]
;
%A = load i32, i32* %X
%B = load i32, i32* %Y
%C = add i32 %A, %B
ret i32 %C
}


define i32 @scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %B) #2 {
; CHECK-LABEL: define {{[^@]+}}@scalar_avx512_legal256_prefer256_call_avx512_legal512_prefer256
; CHECK-SAME: (i32* [[B:%.*]])
; CHECK-NEXT:    [[A:%.*]] = alloca i32
; CHECK-NEXT:    store i32 1, i32* [[A]]
; CHECK-NEXT:    [[A_VAL:%.*]] = load i32, i32* [[A]]
; CHECK-NEXT:    [[B_VAL:%.*]] = load i32, i32* [[B]]
; CHECK-NEXT:    [[C:%.*]] = call i32
@scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32 [[A_VAL]], i32 [[B_VAL]])
; CHECK-NEXT:    ret i32 [[C]]
;
%A = alloca i32
store i32 1, i32* %A
%C = call i32 @scalar_callee_avx512_legal256_prefer256_call_avx512_legal512_prefer256(i32* %A, i32* %B)
ret i32 %C
}


; If the arguments are scalar, its ok to promote.
define internal i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %X, i32*
%Y) #2 {
; CHECK-LABEL: define
{{[^@]+}}@scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (i32 [[X_VAL:%.*]], i32 [[Y_VAL:%.*]])
; CHECK-NEXT:    [[C:%.*]] = add i32 [[X_VAL]], [[Y_VAL]]
; CHECK-NEXT:    ret i32 [[C]]
;
%A = load i32, i32* %X
%B = load i32, i32* %Y
```

```
  %C = add i32 %A, %B
  ret i32 %C
}


define i32 @scalar_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %B) #2 {
; CHECK-LABEL: define {{[^@]+}}@scalar_avx512_legal512_prefer256_call_avx512_legal256_prefer256
; CHECK-SAME: (i32* [[B:%.*]])
; CHECK-NEXT:    [[A:%.*]] = alloca i32
; CHECK-NEXT:    store i32 1, i32* [[A]]
; CHECK-NEXT:    [[A_VAL:%.*]] = load i32, i32* [[A]]
; CHECK-NEXT:    [[B_VAL:%.*]] = load i32, i32* [[B]]
; CHECK-NEXT:    [[C:%.*]] = call i32
@scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32 [[A_VAL]], i32 [[B_VAL]])
; CHECK-NEXT:    ret i32 [[C]]
;
  %A = alloca i32
  store i32 1, i32* %A
  %C = call i32 @scalar_callee_avx512_legal512_prefer256_call_avx512_legal256_prefer256(i32* %A, i32* %B)
  ret i32 %C
}


; Function Attrs: argmemonly nounwind
declare void @llvm.memset.p0i8.i64(i8* nocapture writeonly, i8, i64, i1) #5


attributes #0 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="512" }
attributes #1 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="512" "prefer-vector-width"="256" }
attributes #2 = { inlinehint norecurse nounwind uwtable "target-features"="+avx512vl" "min-legal-vector-
width"="256" "prefer-vector-width"="256" }
attributes #3 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="512"
"prefer-vector-width"="256" }
attributes #4 = { inlinehint norecurse nounwind uwtable "target-features"="+avx2" "min-legal-vector-width"="256"
"prefer-vector-width"="256" }
attributes #5 = { argmemonly nounwind }
```
----
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```
; RUN: opt -mtriple=aarch64-linux-gnu -mattr=+sve -scalarize-masked-mem-intrin -S < %s | FileCheck %s


; Testing that masked scatters operating on scalable vectors that are
; packed in SVE registers are not scalarized.

; CHECK-LABEL: @masked_scatter_nxv4i32(
; CHECK: call void @llvm.masked.scatter.nxv4i32
define void @masked_scatter_nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x i32*> %ptrs, <vscale x 4 x i1> %masks) {
 call void @llvm.masked.scatter.nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x i32*> %ptrs, i32 0, <vscale x 4 x i1> %masks)
 ret void
}


; Testing that masked scatters operating on scalable vectors of FP
; data that is packed in SVE registers are not scalarized.

; CHECK-LABEL: @masked_scatter_nxv2f64(
; CHECK: call void @llvm.masked.scatter.nxv2f64
define void @masked_scatter_nxv2f64(<vscale x 2 x double> %data, <vscale x 2 x double*> %ptrs, <vscale x 2 x i1> %masks) {
 call void @llvm.masked.scatter.nxv2f64(<vscale x 2 x double> %data, <vscale x 2 x double*> %ptrs, i32 0, <vscale x 2 x i1> %masks)
 ret void
}


; Testing that masked scatters operating on scalable vectors of FP
; data that is unpacked in SVE registers are not scalarized.

; CHECK-LABEL: @masked_scatter_nxv2f16(
; CHECK: call void @llvm.masked.scatter.nxv2f16
define void @masked_scatter_nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x half*> %ptrs, <vscale x 2 x i1> %masks) {
 call void @llvm.masked.scatter.nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x half*> %ptrs, i32 0, <vscale x 2 x i1> %masks)
 ret void
}


; Testing that masked scatters operating on 64-bit fixed vectors are
; scalarized because NEON doesn't have support for masked scatter
; instructions.

; CHECK-LABEL: @masked_scatter_v2f32(
; CHECK-NOT: @llvm.masked.scatter.v2f32(
define void @masked_scatter_v2f32(<2 x float> %data, <2 x float*> %ptrs, <2 x i1> %masks) {
```

```
  call void @llvm.masked.scatter.v2f32(<2 x float> %data, <2 x float*> %ptrs, i32 0, <2 x i1> %masks)
  ret void
}


; Testing that masked scatters operating on 128-bit fixed vectors are
; scalarized because NEON doesn't have support for masked scatter
; instructions and because we are not targeting fixed width SVE.


; CHECK-LABEL: @masked_scatter_v4i32(
; CHECK-NOT: @llvm.masked.scatter.v4i32(
define void @masked_scatter_v4i32(<4 x i32> %data, <4 x i32*> %ptrs, <4 x i1> %masks) {
  call void @llvm.masked.scatter.v4i32(<4 x i32> %data, <4 x i32*> %ptrs, i32 0, <4 x i1> %masks)
  ret void
}


declare void @llvm.masked.scatter.nxv4i32(<vscale x 4 x i32> %data, <vscale x 4 x i32*> %ptrs, i32 %align,
<vscale x 4 x i1> %masks)
declare void @llvm.masked.scatter.nxv2f64(<vscale x 2 x double> %data, <vscale x 2 x double*> %ptrs, i32
%align, <vscale x 2 x i1> %masks)
declare void @llvm.masked.scatter.nxv2f16(<vscale x 2 x half> %data, <vscale x 2 x half*> %ptrs, i32 %align,
<vscale x 2 x i1> %masks)
declare void @llvm.masked.scatter.v2f32(<2 x float> %data, <2 x float*> %ptrs, i32 %align, <2 x i1> %masks)
declare void @llvm.masked.scatter.v4i32(<4 x i32> %data, <4 x i32*> %ptrs, i32 %align, <4 x i1> %masks)
```
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```
; NOTE: Assertions have been autogenerated by utils/update_test_checks.py UTC_ARGS: --include-generated-funcs
; RUN: opt -S -verify -iroutliner -ir-outlining-no-cost < %s | FileCheck %s

; This test checks that debug info is recognized as able to be extracted along
; with the other instructions, but is not included in the consolidated function.

define void @function1() !dbg !6 {
entry:
 %a = alloca i32, align 4, !dbg !17
 call void @llvm.dbg.value(metadata i32* %a, metadata !9, metadata !DIExpression()), !dbg !17
 %b = alloca i32, align 4, !dbg !18
 call void @llvm.dbg.value(metadata i32* %b, metadata !11, metadata !DIExpression()), !dbg !18
 %c = alloca i32, align 4, !dbg !19
 call void @llvm.dbg.value(metadata i32* %c, metadata !12, metadata !DIExpression()), !dbg !19
 store i32 2, i32* %a, align 4, !dbg !20
 store i32 3, i32* %b, align 4, !dbg !21
 store i32 4, i32* %c, align 4, !dbg !22
 %al = load i32, i32* %a, align 4, !dbg !23
 call void @llvm.dbg.value(metadata i32 %al, metadata !13, metadata !DIExpression()), !dbg !23
 %bl = load i32, i32* %b, align 4, !dbg !24
 call void @llvm.dbg.value(metadata i32 %bl, metadata !15, metadata !DIExpression()), !dbg !24
```

```
 %cl = load i32, i32* %c, align 4, !dbg !25
 call void @llvm.dbg.value(metadata i32 %cl, metadata !16, metadata !DIExpression()), !dbg !25
 ret void, !dbg !26
}

define void @function2() !dbg !27 {
entry:
 %a = alloca i32, align 4, !dbg !35
 call void @llvm.dbg.value(metadata i32* %a, metadata !29, metadata !DIExpression()), !dbg !35
 %b = alloca i32, align 4, !dbg !36
 call void @llvm.dbg.value(metadata i32* %b, metadata !30, metadata !DIExpression()), !dbg !36
 %c = alloca i32, align 4, !dbg !37
 call void @llvm.dbg.value(metadata i32* %c, metadata !31, metadata !DIExpression()), !dbg !37
 store i32 2, i32* %a, align 4, !dbg !38
 store i32 3, i32* %b, align 4, !dbg !39
 store i32 4, i32* %c, align 4, !dbg !40
 %al = load i32, i32* %a, align 4, !dbg !41
 call void @llvm.dbg.value(metadata i32 %al, metadata !32, metadata !DIExpression()), !dbg !41
 %bl = load i32, i32* %b, align 4, !dbg !42
 call void @llvm.dbg.value(metadata i32 %bl, metadata !33, metadata !DIExpression()), !dbg !42
 %cl = load i32, i32* %c, align 4, !dbg !43
 call void @llvm.dbg.value(metadata i32 %cl, metadata !34, metadata !DIExpression()), !dbg !43
 ret void, !dbg !44
}


; Function Attrs: nounwind readnone speculatable willreturn
declare void @llvm.dbg.value(metadata, metadata, metadata) #0

attributes #0 = { nounwind readnone speculatable willreturn }

!llvm.dbg.cu = !{!0}
!llvm.debugify = !{!3, !4}
!llvm.module.flags = !{!5}

!0 = distinct !DICompileUnit(language: DW_LANG_C, file: !1, producer: "debugify", isOptimized: true,
runtimeVersion: 0, emissionKind: FullDebug, enums: !2)
!1 = !DIFile(filename: "legal-debug.ll", directory: "/")
!2 = !{}
!3 = !{i32 20}
!4 = !{i32 12}
!5 = !{i32 2, !"Debug Info Version", i32 3}
!6 = distinct !DISubprogram(name: "function1", linkageName: "function1", scope: null, file: !1, line: 1, type: !7,
scopeLine: 1, spFlags: DISPFlagDefinition | DISPFlagOptimized, unit: !0, retainedNodes: !8)
!7 = !DISubroutineType(types: !2)
!8 = !{!9, !11, !12, !13, !15, !16}
!9 = !DILocalVariable(name: "1", scope: !6, file: !1, line: 1, type: !10)
!10 = !DIBasicType(name: "ty64", size: 64, encoding: DW_ATE_unsigned)
```

!11 = !DILocalVariable(name: "2", scope: !6, file: !1, line: 2, type: !10)

!12 = !DILocalVariable(name: "3", scope: !6, file: !1, line: 3, type: !10)

!13 = !DILocalVariable(name: "4", scope: !6, file: !1, line: 7, type: !14)

!14 = !DIBasicType(name: "ty32", size: 32, encoding: DW_ATE_unsigned)

!15 = !DILocalVariable(name: "5", scope: !6, file: !1, line: 8, type: !14)

!16 = !DILocalVariable(name: "6", scope: !6, file: !1, line: 9, type: !14)

!17 = !DILocation(line: 1, column: 1, scope: !6)

!18 = !DILocation(line: 2, column: 1, scope: !6)

!19 = !DILocation(line: 3, column: 1, scope: !6)

!20 = !DILocation(line: 4, column: 1, scope: !6)

!21 = !DILocation(line: 5, column: 1, scope: !6)

!22 = !DILocation(line: 6, column: 1, scope: !6)

!23 = !DILocation(line: 7, column: 1, scope: !6)

!24 = !DILocation(line: 8, column: 1, scope: !6)

!25 = !DILocation(line: 9, column: 1, scope: !6)

!26 = !DILocation(line: 10, column: 1, scope: !6)

!27 = distinct !DISubprogram(name: "function2", linkageName: "function2", scope: null, file: !1, line: 11, type: !7, scopeLine: 11, spFlags: DISPFlagDefinition | DISPFlagOptimized, unit: !0, retainedNodes: !28)

!28 = !{!29, !30, !31, !32, !33, !34}

!29 = !DILocalVariable(name: "7", scope: !27, file: !1, line: 11, type: !10)

!30 = !DILocalVariable(name: "8", scope: !27, file: !1, line: 12, type: !10)

!31 = !DILocalVariable(name: "9", scope: !27, file: !1, line: 13, type: !10)

!32 = !DILocalVariable(name: "10", scope: !27, file: !1, line: 17, type: !14)

!33 = !DILocalVariable(name: "11", scope: !27, file: !1, line: 18, type: !14)

!34 = !DILocalVariable(name: "12", scope: !27, file: !1, line: 19, type: !14)

!35 = !DILocation(line: 11, column: 1, scope: !27)

!36 = !DILocation(line: 12, column: 1, scope: !27)

!37 = !DILocation(line: 13, column: 1, scope: !27)

!38 = !DILocation(line: 14, column: 1, scope: !27)

!39 = !DILocation(line: 15, column: 1, scope: !27)

!40 = !DILocation(line: 16, column: 1, scope: !27)

!41 = !DILocation(line: 17, column: 1, scope: !27)

!42 = !DILocation(line: 18, column: 1, scope: !27)

!43 = !DILocation(line: 19, column: 1, scope: !27)

!44 = !DILocation(line: 20, column: 1, scope: !27)

; CHECK-LABEL: @function1(

; CHECK-NEXT: entry:

; CHECK-NEXT: [[A:%.*]] = alloca i32, align 4, !dbg [[DBG17:![0-9]+]]

; CHECK-NEXT: call void @llvm.dbg.value(metadata i32* [[A]], metadata [[META9:![0-9]+]], metadata !DIExpression()), !dbg [[DBG17]]

; CHECK-NEXT: [[B:%.*]] = alloca i32, align 4, !dbg [[DBG18:![0-9]+]]

; CHECK-NEXT: call void @llvm.dbg.value(metadata i32* [[B]], metadata [[META11:![0-9]+]], metadata !DIExpression()), !dbg [[DBG18]]

; CHECK-NEXT: [[C:%.*]] = alloca i32, align 4, !dbg [[DBG19:![0-9]+]]

; CHECK-NEXT: call void @llvm.dbg.value(metadata i32* [[C]], metadata [[META12:![0-9]+]], metadata !DIExpression()), !dbg [[DBG19]]

; CHECK-NEXT: call void @outlined_ir_func_0(i32* [[A]], i32* [[B]], i32* [[C]]), !dbg [[DBG20:![0-9]+]]

; CHECK-NEXT: ret void, !dbg [[DBG21:![0-9]+]]

```
;
;
; CHECK-LABEL: @function2(
; CHECK-NEXT:  entry:
; CHECK-NEXT:    [[A:%.*]] = alloca i32, align 4, !dbg [[DBG30:![0-9]+]]
; CHECK-NEXT:    call void @llvm.dbg.value(metadata i32* [[A]], metadata [[META24:![0-9]+]], metadata
!DIExpression()), !dbg [[DBG30]]
; CHECK-NEXT:    [[B:%.*]] = alloca i32, align 4, !dbg [[DBG31:![0-9]+]]
; CHECK-NEXT:    call void @llvm.dbg.value(metadata i32* [[B]], metadata [[META25:![0-9]+]], metadata
!DIExpression()), !dbg [[DBG31]]
; CHECK-NEXT:    [[C:%.*]] = alloca i32, align 4, !dbg [[DBG32:![0-9]+]]
; CHECK-NEXT:    call void @llvm.dbg.value(metadata i32* [[C]], metadata [[META26:![0-9]+]], metadata
!DIExpression()), !dbg [[DBG32]]
; CHECK-NEXT:    call void @outlined_ir_func_0(i32* [[A]], i32* [[B]], i32* [[C]]), !dbg [[DBG33:![0-9]+]]
; CHECK-NEXT:    ret void, !dbg [[DBG34:![0-9]+]]
;
;
; CHECK: @outlined_ir_func_0(i32* [[TMP0:%.*]], i32* [[TMP1:%.*]], i32*  [[TMP2:%.*]])
; CHECK:       entry_to_outline:
; CHECK-NEXT:    store i32 2, i32* [[TMP0]], align 4
; CHECK-NEXT:    store i32 3, i32* [[TMP1]], align 4
; CHECK-NEXT:    store i32 4, i32* [[TMP2]], align 4
; CHECK-NEXT:    [[AL:%.*]] = load i32, i32* [[TMP0]], align 4
; CHECK-NEXT:    [[BL:%.*]] = load i32, i32* [[TMP1]], align 4
; CHECK-NEXT:    [[CL:%.*]] = load i32, i32* [[TMP2]], align 4
; CHECK-NEXT:    br label [[ENTRY_AFTER_OUTLINE_EXITSTUB:%.*]]
;
```

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  ObjectContainerBSDArchive.cpp

  LINK_LIBS
    lldbCore
    lldbHost
    lldbSymbol
  LINK_COMPONENTS
    Support
  )
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```
; RUN: llc -march=hexagon -hexagon-hvx-widen=32 < %s | FileCheck %s

; Truncating a type-to-be-widenened to a legal type (v8i8).
; Check that this compiles successfully.
; CHECK-LABEL: f0:
; CHECK: dealloc_return

target datalayout = "e-m:e-p:32:32:32-a:0-n16:32-i64:64:64-i32:32:32-i16:16:16-i1:8:8-f32:32:32-f64:64:64-v32:32:32-v64:64:64-v512:512:512-v1024:1024:1024-v2048:2048:2048"
target triple = "hexagon"

define dllexport void @f0(i8* %a0) local_unnamed_addr #0 {
b0:
 %v0 = load i8, i8* undef, align 1
 %v1 = zext i8 %v0 to i16
 %v2 = add i16 0, %v1
 %v3 = icmp sgt i16 %v2, 1
 %v4 = select i1 %v3, i16 %v2, i16 1
 %v5 = udiv i16 -32768, %v4
 %v6 = zext i16 %v5 to i32
 %v7 = insertelement <8 x i32> undef, i32 %v6, i32 0
 %v8 = shufflevector <8 x i32> %v7, <8 x i32> undef, <8 x i32> zeroinitializer
 %v9 = load <8 x i16>, <8 x i16>* undef, align 2
 %v10 = sext <8 x i16> %v9 to <8 x i32>
 %v11 = mul nsw <8 x i32> %v8, %v10
 %v12 = add nsw <8 x i32> %v11, <i32 16384, i32 16384, i32 16384, i32 16384, i32 16384, i32 16384, i32 16384, i32 16384>
 %v13 = lshr <8 x i32> %v12, <i32 15, i32 15, i32 15, i32 15, i32 15, i32 15, i32 15, i32 15>
 %v14 = trunc <8 x i32> %v13 to <8 x i8>
 %v15 = getelementptr inbounds i8, i8* %a0, i32 undef
 %v16 = bitcast i8* %v15 to <8 x i8>*
 store <8 x i8> %v14, <8 x i8>* %v16, align 1
 ret void
```

```
}

attributes #0 = { "target-features"="+hvx,+hvx-length128b" }
; RUN: llc -march=hexagon < %s
; REQUIRES: asserts


; The two loads based on %struct.0, loading two different data types
; cause LSR to assume type "void" for the memory type. This would then
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"

%struct.0 = type { i8*, i8, %union.anon.0 }
%union.anon.0 = type { i8* }

define hidden fastcc void @fred() unnamed_addr #0 {
entry:
 br i1 undef, label %while.end, label %while.body.lr.ph

while.body.lr.ph:                    ; preds = %entry
 br label %while.body

while.body:                          ; preds = %exit.2, %while.body.lr.ph
 %lsr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
 switch i32 undef, label %exit [
   i32 1, label %sw.bb.i
   i32 2, label %sw.bb3.i
 ]

sw.bb.i:                             ; preds = %while.body
 unreachable

sw.bb3.i:                            ; preds = %while.body
 unreachable

exit:                                ; preds = %while.body
 switch i32 undef, label %exit.2 [
   i32 1, label %sw.bb.i17
   i32 2, label %sw.bb3.i20
 ]

sw.bb.i17:                           ; preds = %.exit
 %0 = bitcast %struct.0* %lsr.iv to i32*
 %1 = load i32, i32* %0, align 4
 unreachable

sw.bb3.i20:                          ; preds = %exit
 %2 = bitcast %struct.0* %lsr.iv to i8**
```

```
  %3 = load i8*, i8** %2, align 4
  unreachable

exit.2:                           ; preds = %exit
  %cgep22 = getelementptr %struct.0, %struct.0* %lsr.iv, i32 1
  br label %while.body

while.end:                        ; preds = %entry
  ret void
}

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }
```

LLVM System Interface Library

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```
; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=VEC256,AVX
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+prefer-256-bit | FileCheck %s --check-prefixes=VEC256,AVX512VL256
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,-prefer-256-bit | FileCheck %s --check-prefixes=AVX512VL512
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=VEC256,SKX256
; RUN: opt < %s  -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=SKX512

define void @zext256() "min-legal-vector-width"="256" {
; AVX-LABEL: 'zext256'
; AVX-NEXT:  Cost Model: Found an estimated cost of 4 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX-NEXT:  Cost Model: Found an estimated cost of 5 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; AVX-NEXT:  Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; AVX-NEXT:  Cost Model: Found an estimated cost of 5 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX-NEXT:  Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL256-LABEL: 'zext256'
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 2 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 2 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to
```

<16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; AVX512VL512-LABEL: 'zext256'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; SKX256-LABEL: 'zext256'

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; SKX512-LABEL: 'zext256'

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

%A = zext <8 x i16> undef to <8 x i64>

%B = zext <8 x i32> undef to <8 x i64>

%C = zext <16 x i8> undef to <16 x i32>

%D = zext <16 x i16> undef to <16 x i32>

```
  %E = zext <32 x i8> undef to <32 x i16>
  ret void
}

define void @zext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'zext512'
; AVX-NEXT:  Cost Model: Found an estimated cost of 4 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; AVX-NEXT:  Cost Model: Found an estimated cost of 5 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; AVX-NEXT:  Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %D = zext <16 x i16> undef to <16 x
i32>
; AVX-NEXT:  Cost Model: Found an estimated cost of 5 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX-NEXT:  Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL256-LABEL: 'zext512'
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to
<8 x i64>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to
<8 x i64>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to
<16 x i32>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to
<16 x i32>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to
<32 x i16>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'zext512'
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to
<8 x i64>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to
<8 x i64>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to
<16 x i32>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to
<16 x i32>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to
<32 x i16>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'zext512'
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x
i64>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x
i64>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x
i32>
; SKX256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x
```

i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; SKX512-LABEL: 'zext512'

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

 %A = zext <8 x i16> undef to <8 x i64>

 %B = zext <8 x i32> undef to <8 x i64>

 %C = zext <16 x i8> undef to <16 x i32>

 %D = zext <16 x i16> undef to <16 x i32>

 %E = zext <32 x i8> undef to <32 x i16>

 ret void

}

define void @sext256() "min-legal-vector-width"="256" {

; AVX-LABEL: 'sext256'

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %A = sext <8 x i8> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %B = sext <8 x i16> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %C = sext <8 x i32> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; AVX512VL256-LABEL: 'sext256'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = sext <8 x i8> undef to <8 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = sext <8 x i16> undef to <8 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = sext <16 x i8> undef to <16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to

<32 x i16>
; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'sext256'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'sext256'
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'sext256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
 %A = sext <8 x i8> undef to <8 x i64>
 %B = sext <8 x i16> undef to <8 x i64>

```
%C = sext <8 x i32> undef to <8 x i64>
%D = sext <16 x i8> undef to <16 x i32>
%E = sext <16 x i16> undef to <16 x i32>
%F = sext <32 x i8> undef to <32 x i16>
ret void
}

define void @sext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'sext512'
; AVX-NEXT:  Cost Model: Found an estimated cost of 4 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX-NEXT:  Cost Model: Found an estimated cost of 4 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX-NEXT:  Cost Model: Found an estimated cost of 5 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX-NEXT:  Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX-NEXT:  Cost Model: Found an estimated cost of 5 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX-NEXT:  Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL256-LABEL: 'sext512'
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX512VL256-NEXT:  Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'sext512'
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX512VL512-NEXT:  Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'sext512'
```

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'sext512'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
  %A = sext <8 x i8> undef to <8 x i64>
  %B = sext <8 x i16> undef to <8 x i64>
  %C = sext <8 x i32> undef to <8 x i64>
  %D = sext <16 x i8> undef to <16 x i32>
  %E = sext <16 x i16> undef to <16 x i32>
  %F = sext <32 x i8> undef to <32 x i16>
  ret void
}

define void @trunc256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'trunc256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = trunc <16 x i32> undef to <16 x i8>

; VEC256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; AVX512VL512-LABEL: 'trunc256'
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX512-LABEL: 'trunc256'
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = trunc <8 x i64> undef to <8 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %B = trunc <8 x i64> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %C = trunc <8 x i64> undef to <8 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %D = trunc <16 x i32> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %E = trunc <16 x i32> undef to <16 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %F = trunc <32 x i16> undef to <32 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
  %A = trunc <8 x i64> undef to <8 x i32>
  %B = trunc <8 x i64> undef to <8 x i16>
  %C = trunc <8 x i64> undef to <8 x i8>
  %D = trunc <16 x i32> undef to <16 x i16>
  %E = trunc <16 x i32> undef to <16 x i8>
  %F = trunc <32 x i16> undef to <32 x i8>
  ret void
}

define i32 @zext256_vXi1() "min-legal-vector-width"="256" {
; AVX-LABEL: 'zext256_vXi1'
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = zext <4 x i1> undef to <4 x

i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>
; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL256-LABEL: 'zext256_vXi1'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V2i16 = zext <2 x i1> undef

to <2 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 6 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 12 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 25 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 50 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL512-LABEL: 'zext256_vXi1'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 19 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; SKX256-LABEL: 'zext256_vXi1'

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32

x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>

; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; SKX512-LABEL: 'zext256_vXi1'

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = zext <2 x i1> undef to <2 x i64>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = zext <4 x i1> undef to <4 x i64>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = zext <8 x i1> undef to <8 x i64>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = zext <2 x i1> undef to <2 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = zext <4 x i1> undef to <4 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = zext <8 x i1> undef to <8 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = zext <16 x i1> undef to <16 x i32>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = zext <2 x i1> undef to <2 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = zext <4 x i1> undef to <4 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = zext <8 x i1> undef to <8 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = zext <16 x i1> undef to <16 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = zext <32 x i1> undef to <32 x i16>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = zext <2 x i1> undef to <2 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = zext <4 x i1> undef to <4 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = zext <8 x i1> undef to <8 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = zext <16 x i1> undef to <16 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = zext <32 x i1> undef to <32 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = zext <64 x i1> undef to <64 x i8>

; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

 %V2i64 = zext <2 x i1> undef to <2 x i64>

 %V4i64 = zext <4 x i1> undef to <4 x i64>

 %V8i64 = zext <8 x i1> undef to <8 x i64>

```
%V2i32 = zext <2 x i1> undef to <2 x i32>
%V4i32 = zext <4 x i1> undef to <4 x i32>
%V8i32 = zext <8 x i1> undef to <8 x i32>
%V16i32 = zext <16 x i1> undef to <16 x i32>

%V2i16 = zext <2 x i1> undef to <2 x i16>
%V4i16 = zext <4 x i1> undef to <4 x i16>
%V8i16 = zext <8 x i1> undef to <8 x i16>
%V16i16 = zext <16 x i1> undef to <16 x i16>
%V32i16 = zext <32 x i1> undef to <32 x i16>

%V2i8 = zext <2 x i1> undef to <2 x i8>
%V4i8 = zext <4 x i1> undef to <4 x i8>
%V8i8 = zext <8 x i1> undef to <8 x i8>
%V16i8 = zext <16 x i1> undef to <16 x i8>
%V32i8 = zext <32 x i1> undef to <32 x i8>
%V64i8 = zext <64 x i1> undef to <64 x i8>

ret i32 undef
}

define i32 @sext256_vXi1() "min-legal-vector-width"="256" {
; AVX-LABEL: 'sext256_vXi1'
; AVX-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; AVX-NEXT:  Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; AVX-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; AVX-NEXT:  Cost Model: Found an estimated cost of 4 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; AVX-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; AVX-NEXT:  Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; AVX-NEXT:  Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; AVX-NEXT:  Cost Model: Found an estimated cost of 3 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; AVX-NEXT:  Cost Model: Found an estimated cost of 4 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; AVX-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; AVX-NEXT:  Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; AVX-NEXT:  Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; AVX-NEXT:  Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; AVX-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
```

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL256-LABEL: 'sext256_vXi1'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 20 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V8i8 = sext <8 x i1> undef to

<8 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 21 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 42 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL512-LABEL: 'sext256_vXi1'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX256-LABEL: 'sext256_vXi1'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
; SKX512-LABEL: 'sext256_vXi1'

; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I64 = sext i1 undef to i64
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i64 = sext <2 x i1> undef to <2 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i64 = sext <4 x i1> undef to <4 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i64 = sext <8 x i1> undef to <8 x i64>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I32 = sext i1 undef to i32
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = sext <2 x i1> undef to <2 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i32 = sext <4 x i1> undef to <4 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i32 = sext <8 x i1> undef to <8 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i32 = sext <16 x i1> undef to <16 x i32>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I16 = sext i1 undef to i16
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = sext <2 x i1> undef to <2 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = sext <4 x i1> undef to <4 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i16 = sext <8 x i1> undef to <8 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i16 = sext <16 x i1> undef to <16 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i16 = sext <32 x i1> undef to <32 x i16>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %I8 = sext i1 undef to i8
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = sext <2 x i1> undef to <2 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = sext <4 x i1> undef to <4 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = sext <8 x i1> undef to <8 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V16i8 = sext <16 x i1> undef to <16 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V32i8 = sext <32 x i1> undef to <32 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V64i8 = sext <64 x i1> undef to <64 x i8>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
  %I64 = sext i1 undef to i64
  %V2i64 = sext <2 x i1> undef to <2 x i64>
  %V4i64 = sext <4 x i1> undef to <4 x i64>
  %V8i64 = sext <8 x i1> undef to <8 x i64>

  %I32 = sext i1 undef to i32

```
%V2i32 = sext <2 x i1> undef to <2 x i32>
%V4i32 = sext <4 x i1> undef to <4 x i32>
%V8i32 = sext <8 x i1> undef to <8 x i32>
%V16i32 = sext <16 x i1> undef to <16 x i32>

%I16 = sext i1 undef to i16
%V2i16 = sext <2 x i1> undef to <2 x i16>
%V4i16 = sext <4 x i1> undef to <4 x i16>
%V8i16 = sext <8 x i1> undef to <8 x i16>
%V16i16 = sext <16 x i1> undef to <16 x i16>
%V32i16 = sext <32 x i1> undef to <32 x i16>

%I8 = sext i1 undef to i8
%V2i8 = sext <2 x i1> undef to <2 x i8>
%V4i8 = sext <4 x i1> undef to <4 x i8>
%V8i8 = sext <8 x i1> undef to <8 x i8>
%V16i8 = sext <16 x i1> undef to <16 x i8>
%V32i8 = sext <32 x i1> undef to <32 x i8>
%V64i8 = sext <64 x i1> undef to <64 x i8>

ret i32 undef
}

define i32 @trunc_vXi1() "min-legal-vector-width"="256" {
; AVX-LABEL: 'trunc_vXi1'
; AVX-NEXT:  Cost Model: Found an estimated cost of 0 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>
; AVX-NEXT:  Cost Model: Found an estimated cost of 4 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>
; AVX-NEXT:  Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>
; AVX-NEXT:  Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>
; AVX-NEXT:  Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>
; AVX-NEXT:  Cost Model: Found an estimated cost of 46 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>
; AVX-NEXT:  Cost Model: Found an estimated cost of 1 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>
; AVX-NEXT:  Cost Model: Found an estimated cost of 0 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>
; AVX-NEXT:  Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
; AVX-NEXT:  Cost Model: Found an estimated cost of 8 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
; AVX-NEXT:  Cost Model: Found an estimated cost of 17 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
; AVX-NEXT:  Cost Model: Found an estimated cost of 34 for instruction: %V64i32 = trunc <64 x i32> undef to
```

<64 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 18 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>

; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL256-LABEL: 'trunc_vXi1'

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 22 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 44 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 10 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 20 for instruction: %V64i32 = trunc <64 x i32>

undef to <64 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 16 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 32 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 17 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 34 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>

; AVX512VL256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; AVX512VL512-LABEL: 'trunc_vXi1'

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 22 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 44 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 8 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 14 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 15 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>

; AVX512VL512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; SKX256-LABEL: 'trunc_vXi1'

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 9 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 47 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8

x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>

; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef

;

; SKX512-LABEL: 'trunc_vXi1'

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i64 = trunc <2 x i64> undef to <2 x i1>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i64 = trunc <4 x i64> undef to <4 x i1>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i64 = trunc <8 x i64> undef to <8 x i1>

; SKX512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V16i64 = trunc <16 x i64> undef to <16 x i1>

; SKX512-NEXT: Cost Model: Found an estimated cost of 23 for instruction: %V32i64 = trunc <32 x i64> undef to <32 x i1>

; SKX512-NEXT: Cost Model: Found an estimated cost of 47 for instruction: %V64i64 = trunc <64 x i64> undef to <64 x i1>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i32 = trunc <2 x i32> undef to <2 x i1>

; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i32 = trunc <4 x i32> undef to <4 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i32 = trunc <8 x i32> undef to <8 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i32 = trunc <16 x i32> undef to <16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V32i32 = trunc <32 x i32> undef to <32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 11 for instruction: %V64i32 = trunc <64 x i32> undef to <64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i16 = trunc <2 x i16> undef to <2 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i16 = trunc <4 x i16> undef to <4 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i16 = trunc <8 x i16> undef to <8 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i16 = trunc <16 x i16> undef to <16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i16 = trunc <32 x i16> undef to <32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 5 for instruction: %V64i16 = trunc <64 x i16> undef to <64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V2i8 = trunc <2 x i8> undef to <2 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V4i8 = trunc <4 x i8> undef to <4 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V8i8 = trunc <8 x i8> undef to <8 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V16i8 = trunc <16 x i8> undef to <16 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V32i8 = trunc <32 x i8> undef to <32 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 2 for instruction: %V64i8 = trunc <64 x i8> undef to <64 x i1>
; SKX512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret i32 undef
;
  %V2i64 = trunc <2 x i64> undef to <2 x i1>
  %V4i64 = trunc <4 x i64> undef to <4 x i1>
  %V8i64 = trunc <8 x i64> undef to <8 x i1>
  %V16i64 = trunc <16 x i64> undef to <16 x i1>
  %V32i64 = trunc <32 x i64> undef to <32 x i1>
  %V64i64 = trunc <64 x i64> undef to <64 x i1>

  %V2i32 = trunc <2 x i32> undef to <2 x i1>
  %V4i32 = trunc <4 x i32> undef to <4 x i1>
  %V8i32 = trunc <8 x i32> undef to <8 x i1>
  %V16i32 = trunc <16 x i32> undef to <16 x i1>
  %V32i32 = trunc <32 x i32> undef to <32 x i1>

```
%V64i32 = trunc <64 x i32> undef to <64 x i1>


%V2i16 = trunc <2 x i16> undef to <2 x i1>
%V4i16 = trunc <4 x i16> undef to <4 x i1>
%V8i16 = trunc <8 x i16> undef to <8 x i1>
%V16i16 = trunc <16 x i16> undef to <16 x i1>
%V32i16 = trunc <32 x i16> undef to <32 x i1>
%V64i16 = trunc <64 x i16> undef to <64 x i1>


%V2i8 = trunc <2 x i8> undef to <2 x i1>
%V4i8 = trunc <4 x i8> undef to <4 x i1>
%V8i8 = trunc <8 x i8> undef to <8 x i1>
%V16i8 = trunc <16 x i8> undef to <16 x i1>
%V32i8 = trunc <32 x i8> undef to <32 x i1>
%V64i8 = trunc <64 x i8> undef to <64 x i1>


ret i32 undef
}
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s


define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
; CHECK-LABEL: test_sitofp_fixed:
; CHECK:       ; %bb.0:
; CHECK-NEXT:    sshll2.2d v4, v2, #0
; CHECK-NEXT:    sshll.2d v16, v1, #0
; CHECK-NEXT:    sshll2.2d v5, v0, #0
; CHECK-NEXT:    sshll2.2d v6, v1, #0
; CHECK-NEXT:    sshll2.2d v7, v3, #0
; CHECK-NEXT:    sshll.2d v0, v0, #0
; CHECK-NEXT:    sshll.2d v17, v2, #0
; CHECK-NEXT:    sshll.2d v18, v3, #0
; CHECK-NEXT:    scvtf.2d v1, v5, #6
; CHECK-NEXT:    scvtf.2d v3, v6, #6
; CHECK-NEXT:    scvtf.2d v2, v16, #6
; CHECK-NEXT:    scvtf.2d v5, v4, #6
; CHECK-NEXT:    scvtf.2d v0, v0, #6
; CHECK-NEXT:    scvtf.2d v7, v7, #6
; CHECK-NEXT:    scvtf.2d v4, v17, #6
; CHECK-NEXT:    scvtf.2d v6, v18, #6
; CHECK-NEXT:    ret


%flt = sitofp <16 x i32> %in to <16 x double>
%res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
ret <16 x double> %res
}
```

```
; This one is small enough to satisfy isSimple, but still illegally large.
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:
; CHECK:       ; %bb.0:
; CHECK-NEXT:    scvtf.2d v0, v0, #6
; CHECK-NEXT:    scvtf.2d v1, v1, #6
; CHECK-NEXT:    ret



  %flt = sitofp <4 x i64> %in to <4 x double>
  %res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
  ret <4 x double> %res
}
```

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```
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 -mattr=prefer-256-bit,avx512vbmi | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; Make sure CPUs default to prefer-256-bit. avx512vnni isn't interesting as it just adds an isel peephole for vpmaddwd+vpaddd
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=skylake-avx512 | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cascadelake | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=cooperlake | FileCheck %s --check-prefixes=CHECK,CHECK-AVX512
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mcpu=cannonlake | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-client | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=icelake-server | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=-avx512vnni -mcpu=tigerlake | FileCheck %s --check-prefixes=CHECK,CHECK-VBMI


; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

define dso_local void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" {
; CHECK-LABEL: add256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vpaddd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:    vpaddd (%rsi), %ymm0, %ymm0
; CHECK-NEXT:    vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:    vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %d = load <16 x i32>, <16 x i32>* %a
  %e = load <16 x i32>, <16 x i32>* %b
  %f = add <16 x i32> %d, %e
  store <16 x i32> %f, <16 x i32>* %c
  ret void
}
```

```
define dso_local void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-
width"="512" {
; CHECK-LABEL: add512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:    vpaddd (%rsi), %zmm0, %zmm0
; CHECK-NEXT:    vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %d = load <16 x i32>, <16 x i32>* %a
 %e = load <16 x i32>, <16 x i32>* %b
 %f = add <16 x i32> %d, %e
 store <16 x i32> %f, <16 x i32>* %c
 ret void
}


define dso_local void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" {
; CHECK-LABEL: avg_v64i8_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rsi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT:    vpavgb (%rdi), %ymm0, %ymm0
; CHECK-NEXT:    vpavgb 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT:    vmovdqu %ymm1, (%rax)
; CHECK-NEXT:    vmovdqu %ymm0, (%rax)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %1 = load <64 x i8>, <64 x i8>* %a
 %2 = load <64 x i8>, <64 x i8>* %b
 %3 = zext <64 x i8> %1 to <64 x i32>
 %4 = zext <64 x i8> %2 to <64 x i32>
 %5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
 %6 = add nuw nsw <64 x i32> %5, %4
 %7 = lshr <64 x i32> %6, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
 %8 = trunc <64 x i32> %7 to <64 x i8>
 store <64 x i8> %8, <64 x i8>* undef, align 4
 ret void
}



define dso_local void @avg_v64i8_512(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="512" {
; CHECK-LABEL: avg_v64i8_512:
```

; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rsi), %zmm0
; CHECK-NEXT: vpavgb (%rdi), %zmm0, %zmm0
; CHECK-NEXT: vmovdqu64 %zmm0, (%rax)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
 %1 = load <64 x i8>, <64 x i8>* %a
 %2 = load <64 x i8>, <64 x i8>* %b
 %3 = zext <64 x i8> %1 to <64 x i32>
 %4 = zext <64 x i8> %2 to <64 x i32>
 %5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1>
 %6 = add nuw nsw <64 x i32> %5, %4
 %7 = lshr <64 x i32> %6, <i32 1, i32 1>
 %8 = trunc <64 x i32> %7 to <64 x i8>
 store <64 x i8> %8, <64 x i8>* undef, align 4
 ret void
}

define dso_local void @pmaddwd_32_256(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="256" {
; CHECK-LABEL: pmaddwd_32_256:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vpmaddwd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT: vpmaddwd (%rsi), %ymm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
 %A = load <32 x i16>, <32 x i16>* %APtr
 %B = load <32 x i16>, <32 x i16>* %BPtr
 %a = sext <32 x i16> %A to <32 x i32>
 %b = sext <32 x i16> %B to <32 x i32>
 %m = mul nsw <32 x i32> %a, %b
 %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
 %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
 %ret = add <16 x i32> %odd, %even
 store <16 x i32> %ret, <16 x i32>* %CPtr
 ret void

```
}

define dso_local void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-
legal-vector-width"="512" {
; CHECK-LABEL: pmaddwd_32_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:    vpmaddwd (%rsi), %zmm0, %zmm0
; CHECK-NEXT:    vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %A = load <32 x i16>, <32 x i16>* %APtr
  %B = load <32 x i16>, <32 x i16>* %BPtr
  %a = sext <32 x i16> %A to <32 x i32>
  %b = sext <32 x i16> %B to <32 x i32>
  %m = mul nsw <32 x i32> %a, %b
  %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
  %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32
13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
  %ret = add <16 x i32> %odd, %even
  store <16 x i32> %ret, <16 x i32>* %CPtr
  ret void
}


define dso_local void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-
vector-width"="256" {
; CHECK-LABEL: psubus_64i8_max_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vpsubusb 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:    vpsubusb (%rsi), %ymm0, %ymm0
; CHECK-NEXT:    vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:    vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %x = load <64 x i8>, <64 x i8>* %xptr
  %y = load <64 x i8>, <64 x i8>* %yptr
  %cmp = icmp ult <64 x i8> %x, %y
  %max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
  %res = sub <64 x i8> %max, %y
  store <64 x i8> %res, <64 x i8>* %zptr
  ret void
}


define dso_local void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-
vector-width"="512" {
```

```
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:    vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT:    vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %x = load <64 x i8>, <64 x i8>* %xptr
  %y = load <64 x i8>, <64 x i8>* %yptr
  %cmp = icmp ult <64 x i8> %x, %y
  %max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
  %res = sub <64 x i8> %max, %y
  store <64 x i8> %res, <64 x i8>* %zptr
  ret void
}

define dso_local i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
; CHECK-LABEL: _Z9test_charPcS_i_256:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    movl %edx, %eax
; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:    xorl %ecx, %ecx
; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:    vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB8_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:    vpmovsxbw 16(%rdi,%rcx), %ymm3
; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %ymm4
; CHECK-NEXT:    vpmovsxbw 16(%rsi,%rcx), %ymm5
; CHECK-NEXT:    vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-NEXT:    vpaddd %ymm2, %ymm3, %ymm2
; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %ymm3
; CHECK-NEXT:    vpmaddwd %ymm4, %ymm3, %ymm3
; CHECK-NEXT:    vpaddd %ymm1, %ymm3, %ymm1
; CHECK-NEXT:    addq $32, %rcx
; CHECK-NEXT:    cmpq %rcx, %rax
; CHECK-NEXT:    jne .LBB8_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm1
; CHECK-NEXT:    vpaddd %ymm0, %ymm2, %ymm0
; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,1,1]
```

```
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vmovd %xmm0, %eax
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
entry:
 %3 = zext i32 %2 to i64
 br label %vector.body


vector.body:
 %index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
 %vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
 %4 = getelementptr inbounds i8, i8* %0, i64 %index
 %5 = bitcast i8* %4 to <32 x i8>*
 %wide.load = load <32 x i8>, <32 x i8>* %5, align 1
 %6 = sext <32 x i8> %wide.load to <32 x i32>
 %7 = getelementptr inbounds i8, i8* %1, i64 %index
 %8 = bitcast i8* %7 to <32 x i8>*
 %wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
 %9 = sext <32 x i8> %wide.load14 to <32 x i32>
 %10 = mul nsw <32 x i32> %9, %6
 %11 = add nsw <32 x i32> %10, %vec.phi
 %index.next = add i64 %index, 32
 %12 = icmp eq i64 %index.next, %3
 br i1 %12, label %middle.block, label %vector.body


middle.block:
 %rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef>
 %bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
 %rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
 %rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
 %rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
 %rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
```

```llvm
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
 %13 = extractelement <32 x i32> %bin.rdx20, i32 0
 ret i32 %13
}

define dso_local i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-
vector-width"="512" {
; CHECK-LABEL: _Z9test_charPcS_i_512:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    movl %edx, %eax
; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:    xorl %ecx, %ecx
; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB9_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %zmm3
; CHECK-NEXT:    vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-NEXT:    vpaddd %zmm1, %zmm2, %zmm1
; CHECK-NEXT:    addq $32, %rcx
; CHECK-NEXT:    cmpq %rcx, %rax
; CHECK-NEXT:    jne .LBB9_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:    vpaddd %zmm0, %zmm1, %zmm0
; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,1,1]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vmovd %xmm0, %eax
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
entry:
 %3 = zext i32 %2 to i64
 br label %vector.body

vector.body:
 %index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
 %vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
 %4 = getelementptr inbounds i8, i8* %0, i64 %index
 %5 = bitcast i8* %4 to <32 x i8>*
 %wide.load = load <32 x i8>, <32 x i8>* %5, align 1
```

```llvm
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body

middle.block:
 %rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef>
 %bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
 %rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
 %rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
 %rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
 %rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
 %13 = extractelement <32 x i32> %bin.rdx20, i32 0
 ret i32 %13
}

@a = dso_local global [1024 x i8] zeroinitializer, align 16
@b = dso_local global [1024 x i8] zeroinitializer, align 16

define dso_local i32 @sad_16i8_256() "min-legal-vector-width"="256" {
; CHECK-LABEL: sad_16i8_256:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
```

```
; CHECK-NEXT:    movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB10_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:    vmovdqu a+1024(%rax), %xmm2
; CHECK-NEXT:    vpsadbw b+1024(%rax), %xmm2, %xmm2
; CHECK-NEXT:    vpaddd %ymm1, %ymm2, %ymm1
; CHECK-NEXT:    addq $4, %rax
; CHECK-NEXT:    jne .LBB10_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,2,3]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,1,1]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vmovd %xmm0, %eax
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
entry:
 br label %vector.body

vector.body:
 %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
 %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
 %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
 %1 = bitcast i8* %0 to <16 x i8>*
 %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
 %2 = zext <16 x i8> %wide.load to <16 x i32>
 %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
 %4 = bitcast i8* %3 to <16 x i8>*
 %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
 %5 = zext <16 x i8> %wide.load1 to <16 x i32>
 %6 = sub nsw <16 x i32> %2, %5
 %7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
 %8 = sub nsw <16 x i32> zeroinitializer, %6
 %9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
 %10 = add nsw <16 x i32> %9, %vec.phi
 %index.next = add i64 %index, 4
 %11 = icmp eq i64 %index.next, 1024
 br i1 %11, label %middle.block, label %vector.body

middle.block:
 %rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32
13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
```

```
 %bin.rdx = add <16 x i32> %10, %rdx.shuf
 %rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32
 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
 i32 undef>
 %bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
 %rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32
 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
 i32 undef, i32 undef>
 %bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
 %rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32
 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
 i32 undef, i32 undef>
 %bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
 %12 = extractelement <16 x i32> %bin.rdx4, i32 0
 ret i32 %12
 }


 define dso_local i32 @sad_16i8_512() "min-legal-vector-width"="512" {
 ; CHECK-LABEL: sad_16i8_512:
 ; CHECK:       # %bb.0: # %entry
 ; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
 ; CHECK-NEXT:    movq $-1024, %rax # imm = 0xFC00
 ; CHECK-NEXT:    .p2align 4, 0x90
 ; CHECK-NEXT:  .LBB11_1: # %vector.body
 ; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
 ; CHECK-NEXT:    vmovdqu a+1024(%rax), %xmm1
 ; CHECK-NEXT:    vpsadbw b+1024(%rax), %xmm1, %xmm1
 ; CHECK-NEXT:    vpaddd %zmm0, %zmm1, %zmm0
 ; CHECK-NEXT:    addq $4, %rax
 ; CHECK-NEXT:    jne .LBB11_1
 ; CHECK-NEXT:  # %bb.2: # %middle.block
 ; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm1
 ; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
 ; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
 ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
 ; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,2,3]
 ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
 ; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,1,1]
 ; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
 ; CHECK-NEXT:    vmovd %xmm0, %eax
 ; CHECK-NEXT:    vzeroupper
 ; CHECK-NEXT:    retq
 entry:
 br label %vector.body

 vector.body:
 %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
 %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
```

```
%0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
%1 = bitcast i8* %0 to <16 x i8>*
%wide.load = load <16 x i8>, <16 x i8>* %1, align 4
%2 = zext <16 x i8> %wide.load to <16 x i32>
%3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
%4 = bitcast i8* %3 to <16 x i8>*
%wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
%5 = zext <16 x i8> %wide.load1 to <16 x i32>
%6 = sub nsw <16 x i32> %2, %5
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1>
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

middle.block:
 %rdx.shuf = shufflevector <16 x i32> %10, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx = add <16 x i32> %10, %rdx.shuf
 %rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
 %rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
 %rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
 %12 = extractelement <16 x i32> %bin.rdx4, i32 0
 ret i32 %12
}

define dso_local void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm1
; CHECK-NEXT:    vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT:    vmovaps %ymm1, (%rdi)
```

```
; CHECK-NEXT:    vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %mask = icmp slt <16 x i16> %a, zeroinitializer
 %1 = sitofp <16 x i1> %mask to <16 x float>
 store <16 x float> %1, <16 x float>* %res
 ret void
}


define dso_local void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %mask = icmp slt <16 x i16> %a, zeroinitializer
 %1 = sitofp <16 x i1> %mask to <16 x float>
 store <16 x float> %1, <16 x float>* %res
 ret void
}


define dso_local void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f64_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT:    vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT:    vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT:    vmovaps %ymm3, (%rdi)
; CHECK-NEXT:    vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT:    vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %mask = icmp slt <16 x i16> %a, zeroinitializer
 %1 = sitofp <16 x i1> %mask to <16 x double>
 store <16 x double> %1, <16 x double>* %res
 ret void
}
```

```
define dso_local void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f64_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:    vmovaps %zmm1, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = sitofp <16 x i1> %mask to <16 x double>
  store <16 x double> %1, <16 x double>* %res
  ret void
}

define dso_local void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f32_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT:    vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm1
; CHECK-NEXT:    vpsrld $31, %ymm1, %ymm1
; CHECK-NEXT:    vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT:    vmovaps %ymm1, (%rdi)
; CHECK-NEXT:    vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = uitofp <16 x i1> %mask to <16 x float>
  store <16 x float> %1, <16 x float>* %res
  ret void
}

define dso_local void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f32_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT:    vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, (%rdi)
```

```
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %mask = icmp slt <16 x i16> %a, zeroinitializer
 %1 = uitofp <16 x i1> %mask to <16 x float>
 store <16 x float> %1, <16 x float>* %res
 ret void
}

define dso_local void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f64_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm2
; CHECK-NEXT:    vpsrld $31, %ymm2, %ymm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT:    vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT:    vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT:    vmovaps %ymm3, (%rdi)
; CHECK-NEXT:    vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT:    vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %mask = icmp slt <16 x i16> %a, zeroinitializer
 %1 = uitofp <16 x i1> %mask to <16 x double>
 store <16 x double> %1, <16 x double>* %res
 ret void
}

define dso_local void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f64_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:    vmovaps %zmm1, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
```

```
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = uitofp <16 x i1> %mask to <16 x double>
store <16 x double> %1, <16 x double>* %res
ret void
}

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="256" {
; CHECK-LABEL: test_16f32toub_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:    vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:    vpmovd2m %ymm1, %k0
; CHECK-NEXT:    vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:    vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:    vpmovd2m %ymm1, %k1
; CHECK-NEXT:    kunpckbw %k0, %k1, %k1
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:    retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {
; CHECK-LABEL: test_16f32toub_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:    vpslld $31, %zmm1, %zmm1
; CHECK-NEXT:    vpmovd2m %zmm1, %k1
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:    retq
%a = load <16 x float>, <16 x float>* %ptr
%mask = fptoui <16 x float> %a to <16 x i1>
%select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="256" {
; CHECK-LABEL: test_16f32tosb_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:    vpmovd2m %ymm1, %k0
; CHECK-NEXT:    vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:    vpmovd2m %ymm1, %k1
```

```
; CHECK-NEXT:    kunpckbw %k0, %k1, %k1
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:    retq
  %a = load <16 x float>, <16 x float>* %ptr
  %mask = fptosi <16 x float> %a to <16 x i1>
  %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
  ret <16 x i16> %select
}


define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {
; CHECK-LABEL: test_16f32tosb_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:    vpmovd2m %zmm1, %k1
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:    retq
  %a = load <16 x float>, <16 x float>* %ptr
  %mask = fptosi <16 x float> %a to <16 x i1>
  %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
  ret <16 x i16> %select
}


define dso_local void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: mul256:
; CHECK-AVX512:       # %bb.0:
; CHECK-AVX512-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-AVX512-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-AVX512-NEXT:    vmovdqa (%rsi), %ymm2
; CHECK-AVX512-NEXT:    vmovdqa 32(%rsi), %ymm3
; CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm4 =
ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm5 =
ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT:    vpmullw %ymm4, %ymm5, %ymm4
; CHECK-AVX512-NEXT:    vmovdqa {{.*#+}} ymm5 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255]
; CHECK-AVX512-NEXT:    vpand %ymm5, %ymm4, %ymm4
; CHECK-AVX512-NEXT:    vpunpcklbw {{.*#+}} ymm3 =
ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT:    vpunpcklbw {{.*#+}} ymm1 =
ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT:    vpmullw %ymm3, %ymm1, %ymm1
; CHECK-AVX512-NEXT:    vpand %ymm5, %ymm1, %ymm1
; CHECK-AVX512-NEXT:    vpackuswb %ymm4, %ymm1, %ymm1
; CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm3 =
ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm4 =
```

ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-AVX512-NEXT: vpmullw %ymm3, %ymm4, %ymm3
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm3, %ymm3
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm2 =
ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-AVX512-NEXT: vpmullw %ymm2, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vpand %ymm5, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vpackuswb %ymm3, %ymm0, %ymm0
; CHECK-AVX512-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-AVX512-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-AVX512-NEXT: vzeroupper
; CHECK-AVX512-NEXT: retq
;
; CHECK-VBMI-LABEL: mul256:
; CHECK-VBMI: # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-VBMI-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-VBMI-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm3[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm5 =
ymm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm3 =
ymm3[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm1 =
ymm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT: vpmullw %ymm3, %ymm1, %ymm1
; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm3 =
[0,2,4,6,8,10,12,14,32,34,36,38,40,42,44,46,16,18,20,22,24,26,28,30,48,50,52,54,56,58,60,62]
; CHECK-VBMI-NEXT: vpermt2b %ymm4, %ymm3, %ymm1
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm2[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm5 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-VBMI-NEXT: vpmullw %ymm4, %ymm5, %ymm4
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm2 =
ymm2[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-VBMI-NEXT: vpmullw %ymm2, %ymm0, %ymm0
; CHECK-VBMI-NEXT: vpermt2b %ymm4, %ymm3, %ymm0
; CHECK-VBMI-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-VBMI-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-VBMI-NEXT: vzeroupper

```
; CHECK-VBMI-NEXT:    retq
  %d = load <64 x i8>, <64 x i8>* %a
  %e = load <64 x i8>, <64 x i8>* %b
  %f = mul <64 x i8> %d, %e
  store <64 x i8> %f, <64 x i8>* %c
  ret void
}

define dso_local void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" {
; CHECK-AVX512-LABEL: mul512:
; CHECK-AVX512:       # %bb.0:
; CHECK-AVX512-NEXT:    vmovdqa64 (%rdi), %zmm0
; CHECK-AVX512-NEXT:    vmovdqa64 (%rsi), %zmm1
; CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} zmm2 =
zmm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} zmm3 =
zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-AVX512-NEXT:    vpmullw %zmm2, %zmm3, %zmm2
; CHECK-AVX512-NEXT:    vmovdqa64 {{.*#+}} zmm3 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,2
55,255,255,255,255,255]
; CHECK-AVX512-NEXT:    vpandq %zmm3, %zmm2, %zmm2
; CHECK-AVX512-NEXT:    vpunpcklbw {{.*#+}} zmm1 =
zmm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-AVX512-NEXT:    vpunpcklbw {{.*#+}} zmm0 =
zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-AVX512-NEXT:    vpmullw %zmm1, %zmm0, %zmm0
; CHECK-AVX512-NEXT:    vpandq %zmm3, %zmm0, %zmm0
; CHECK-AVX512-NEXT:    vpackuswb %zmm2, %zmm0, %zmm0
; CHECK-AVX512-NEXT:    vmovdqa64 %zmm0, (%rdx)
; CHECK-AVX512-NEXT:    vzeroupper
; CHECK-AVX512-NEXT:    retq
;
; CHECK-VBMI-LABEL: mul512:
; CHECK-VBMI:       # %bb.0:
; CHECK-VBMI-NEXT:    vmovdqa64 (%rdi), %zmm0
; CHECK-VBMI-NEXT:    vmovdqa64 (%rsi), %zmm1
; CHECK-VBMI-NEXT:    vpunpckhbw {{.*#+}} zmm2 =
zmm1[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:    vpunpckhbw {{.*#+}} zmm3 =
zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-VBMI-NEXT:    vpmullw %zmm2, %zmm3, %zmm2
```

; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} zmm1 =
zmm1[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} zmm0 =
zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,3
6,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]
; CHECK-VBMI-NEXT: vpmullw %zmm1, %zmm0, %zmm0
; CHECK-VBMI-NEXT: vmovdqa64 {{.*#+}} zmm1 =
[0,2,4,6,8,10,12,14,64,66,68,70,72,74,76,78,16,18,20,22,24,26,28,30,80,82,84,86,88,90,92,94,32,34,36,38,40,42,44,
46,96,98,100,102,104,106,108,110,48,50,52,54,56,58,60,62,112,114,116,118,120,122,124,126]
; CHECK-VBMI-NEXT: vpermi2b %zmm2, %zmm0, %zmm1
; CHECK-VBMI-NEXT: vmovdqa64 %zmm1, (%rdx)
; CHECK-VBMI-NEXT: vzeroupper
; CHECK-VBMI-NEXT: retq
  %d = load <64 x i8>, <64 x i8>* %a
  %e = load <64 x i8>, <64 x i8>* %b
  %f = mul <64 x i8> %d, %e
  store <64 x i8> %f, <64 x i8>* %c
  ret void
}

; This threw an assertion at one point.
define <4 x i32> @mload_v4i32(<4 x i32> %trigger, <4 x i32>* %addr, <4 x i32> %dst) "min-legal-vector-
width"="256" {
; CHECK-LABEL: mload_v4i32:
; CHECK: # %bb.0:
; CHECK-NEXT: vptestnmd %xmm0, %xmm0, %k1
; CHECK-NEXT: vpblendmd (%rdi), %xmm1, %xmm0 {%k1}
; CHECK-NEXT: retq
  %mask = icmp eq <4 x i32> %trigger, zeroinitializer
  %res = call <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>* %addr, i32 4, <4 x i1> %mask, <4 x i32>
%dst)
  ret <4 x i32> %res
}
declare <4 x i32> @llvm.masked.load.v4i32.p0v4i32(<4 x i32>*, i32, <4 x i1>, <4 x i32>)

define <16 x i32> @trunc_v16i64_v16i32(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i32:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rdi), %ymm0
; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT: vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT: vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT: vpmovqd %ymm0, %xmm0
; CHECK-NEXT: vpmovqd %ymm1, %xmm1
; CHECK-NEXT: vinserti128 $1, %xmm1, %ymm0, %ymm0
; CHECK-NEXT: vpmovqd %ymm2, %xmm1
; CHECK-NEXT: vpmovqd %ymm3, %xmm2

```
; CHECK-NEXT:    vinserti128 $1, %xmm2, %ymm1, %ymm1
; CHECK-NEXT:    retq
 %a = load <16 x i64>, <16 x i64>* %x
 %b = trunc <16 x i64> %a to <16 x i32>
 ret <16 x i32> %b
}


define <16 x i8> @trunc_v16i64_v16i8(<16 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i64_v16i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vmovdqa 64(%rdi), %ymm2
; CHECK-NEXT:    vmovdqa 96(%rdi), %ymm3
; CHECK-NEXT:    vpmovqb %ymm3, %xmm3
; CHECK-NEXT:    vpmovqb %ymm2, %xmm2
; CHECK-NEXT:    vpunpckldq {{.*#+}} xmm2 = xmm2[0],xmm3[0],xmm2[1],xmm3[1]
; CHECK-NEXT:    vpmovqb %ymm1, %xmm1
; CHECK-NEXT:    vpmovqb %ymm0, %xmm0
; CHECK-NEXT:    vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT:    vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm2[0]
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %a = load <16 x i64>, <16 x i64>* %x
 %b = trunc <16 x i64> %a to <16 x i8>
 ret <16 x i8> %b
}


define <16 x i8> @trunc_v16i32_v16i8(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vpmovdb %ymm1, %xmm1
; CHECK-NEXT:    vpmovdb %ymm0, %xmm0
; CHECK-NEXT:    vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0]
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %a = load <16 x i32>, <16 x i32>* %x
 %b = trunc <16 x i32> %a to <16 x i8>
 ret <16 x i8> %b
}


define <8 x i8> @trunc_v8i64_v8i8(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
```

```
; CHECK-NEXT:    vpmovqb %ymm1, %xmm1
; CHECK-NEXT:    vpmovqb %ymm0, %xmm0
; CHECK-NEXT:    vpunpckldq {{.*#+}} xmm0 = xmm0[0],xmm1[0],xmm0[1],xmm1[1]
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %a = load <8 x i64>, <8 x i64>* %x
  %b = trunc <8 x i64> %a to <8 x i8>
  ret <8 x i8> %b
}

define <8 x i16> @trunc_v8i64_v8i16(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i16:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vpmovqw %ymm1, %xmm1
; CHECK-NEXT:    vpmovqw %ymm0, %xmm0
; CHECK-NEXT:    vpunpcklqdq {{.*#+}} xmm0 = xmm0[0],xmm1[0]
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %a = load <8 x i64>, <8 x i64>* %x
  %b = trunc <8 x i64> %a to <8 x i16>
  ret <8 x i16> %b
}

define <8 x i32> @trunc_v8i64_v8i32_zeroes(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i32_zeroes:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpsrlq $48, 32(%rdi), %ymm0
; CHECK-NEXT:    vpsrlq $48, (%rdi), %ymm1
; CHECK-NEXT:    vpackusdw %ymm0, %ymm1, %ymm0
; CHECK-NEXT:    vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT:    retq
  %a = load <8 x i64>, <8 x i64>* %x
  %b = lshr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
  %c = trunc <8 x i64> %b to <8 x i32>
  ret <8 x i32> %c
}

define <16 x i16> @trunc_v16i32_v16i16_zeroes(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i16_zeroes:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm1
; CHECK-NEXT:    vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
; CHECK-NEXT:    vpermi2w 32(%rdi), %ymm1, %ymm0
; CHECK-NEXT:    retq
  %a = load <16 x i32>, <16 x i32>* %x
  %b = lshr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32
```

```
16, i32 16, i32 16, i32 16, i32 16>
 %c = trunc <16 x i32> %b to <16 x i16>
 ret <16 x i16> %c
}


define <32 x i8> @trunc_v32i16_v32i8_zeroes(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_zeroes:
; CHECK-AVX512:       # %bb.0:
; CHECK-AVX512-NEXT:    vpsrlw $8, 32(%rdi), %ymm0
; CHECK-AVX512-NEXT:    vpsrlw $8, (%rdi), %ymm1
; CHECK-AVX512-NEXT:    vpackuswb %ymm0, %ymm1, %ymm0
; CHECK-AVX512-NEXT:    vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-AVX512-NEXT:    retq
;
; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_zeroes:
; CHECK-VBMI:       # %bb.0:
; CHECK-VBMI-NEXT:    vmovdqa (%rdi), %ymm1
; CHECK-VBMI-NEXT:    vmovdqa {{.*#+}} ymm0 =
[1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
; CHECK-VBMI-NEXT:    vpermi2b 32(%rdi), %ymm1, %ymm0
; CHECK-VBMI-NEXT:    retq
 %a = load <32 x i16>, <32 x i16>* %x
 %b = lshr <32 x i16> %a, <i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8,
i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8, i16 8>
 %c = trunc <32 x i16> %b to <32 x i8>
 ret <32 x i8> %c
}


define <8 x i32> @trunc_v8i64_v8i32_sign(<8 x i64>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v8i64_v8i32_sign:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpsraq $48, 32(%rdi), %ymm0
; CHECK-NEXT:    vpsraq $48, (%rdi), %ymm1
; CHECK-NEXT:    vpmovqd %ymm1, %xmm1
; CHECK-NEXT:    vpmovqd %ymm0, %xmm0
; CHECK-NEXT:    vinserti128 $1, %xmm0, %ymm1, %ymm0
; CHECK-NEXT:    retq
 %a = load <8 x i64>, <8 x i64>* %x
 %b = ashr <8 x i64> %a, <i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48, i64 48>
 %c = trunc <8 x i64> %b to <8 x i32>
 ret <8 x i32> %c
}


define <16 x i16> @trunc_v16i32_v16i16_sign(<16 x i32>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_v16i32_v16i16_sign:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm1
; CHECK-NEXT:    vmovdqa {{.*#+}} ymm0 = [1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31]
```

; CHECK-NEXT: vpermi2w 32(%rdi), %ymm1, %ymm0
; CHECK-NEXT: retq
 %a = load <16 x i32>, <16 x i32>* %x
 %b = ashr <16 x i32> %a, <i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16, i32 16>
 %c = trunc <16 x i32> %b to <16 x i16>
 ret <16 x i16> %c
 }

define <32 x i8> @trunc_v32i16_v32i8_sign(<32 x i16>* %x) nounwind "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: trunc_v32i16_v32i8_sign:
; CHECK-AVX512:   # %bb.0:
; CHECK-AVX512-NEXT: vpsrlw $8, 32(%rdi), %ymm0
; CHECK-AVX512-NEXT: vpsrlw $8, (%rdi), %ymm1
; CHECK-AVX512-NEXT: vpackuswb %ymm0, %ymm1, %ymm0
; CHECK-AVX512-NEXT: vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-AVX512-NEXT: retq
;
; CHECK-VBMI-LABEL: trunc_v32i16_v32i8_sign:
; CHECK-VBMI: # %bb.0:
; CHECK-VBMI-NEXT: vmovdqa (%rdi), %ymm1
; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm0 =
[1,3,5,7,9,11,13,15,17,19,21,23,25,27,29,31,33,35,37,39,41,43,45,47,49,51,53,55,57,59,61,63]
; CHECK-VBMI-NEXT: vpermi2b 32(%rdi), %ymm1, %ymm0
; CHECK-VBMI-NEXT: retq
 %a = load <32 x i16>, <32 x i16>* %x
 %b = ashr <32 x i16> %a, <i16 8, i16 8>
 %c = trunc <32 x i16> %b to <32 x i8>
 ret <32 x i8> %c
 }

define dso_local void @zext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: zext_v16i8_v16i64:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovzxbw {{.*#+}} ymm1 =
xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zero,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xmm0[15],zero
; CHECK-NEXT: vpshufd {{.*#+}} xmm2 = xmm1[2,3,2,3]
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm2 =
xmm2[0],zero,zero,zero,xmm2[1],zero,zero,zero,xmm2[2],zero,zero,zero,xmm2[3],zero,zero,zero
; CHECK-NEXT: vextracti128 $1, %ymm1, %xmm1
; CHECK-NEXT: vpshufd {{.*#+}} xmm3 = xmm1[2,3,2,3]
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm3 =
xmm3[0],zero,zero,zero,xmm3[1],zero,zero,zero,xmm3[2],zero,zero,zero,xmm3[3],zero,zero,zero
; CHECK-NEXT: vpmovzxwq {{.*#+}} ymm1 =

xmm1[0],zero,zero,zero,xmm1[1],zero,zero,zero,xmm1[2],zero,zero,zero,xmm1[3],zero,zero,zero

; CHECK-NEXT: vpmovzxbq {{.*#+}} ymm0 =
xmm0[0],zero,zero,zero,zero,zero,zero,zero,xmm0[1],zero,zero,zero,zero,zero,zero,zero,xmm0[2],zero,zero,zero,zero,zero,zero,zero,xmm0[3],zero,zero,zero,zero,zero,zero,zero

; CHECK-NEXT: vmovdqa %ymm0, (%rdi)
; CHECK-NEXT: vmovdqa %ymm1, 64(%rdi)
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT: vmovdqa %ymm2, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
 %a = zext <16 x i8> %x to <16 x i64>
 store <16 x i64> %a, <16 x i64>* %y
 ret void
}

define dso_local void @sext_v16i8_v16i64(<16 x i8> %x, <16 x i64>* %y) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: sext_v16i8_v16i64:
; CHECK: # %bb.0:
; CHECK-NEXT: vpmovsxbw %xmm0, %ymm1
; CHECK-NEXT: vpshufd {{.*#+}} xmm2 = xmm1[2,3,2,3]
; CHECK-NEXT: vpmovsxwq %xmm2, %ymm2
; CHECK-NEXT: vextracti128 $1, %ymm1, %xmm1
; CHECK-NEXT: vpshufd {{.*#+}} xmm3 = xmm1[2,3,2,3]
; CHECK-NEXT: vpmovsxwq %xmm3, %ymm3
; CHECK-NEXT: vpmovsxwq %xmm1, %ymm1
; CHECK-NEXT: vpmovsxbq %xmm0, %ymm0
; CHECK-NEXT: vmovdqa %ymm0, (%rdi)
; CHECK-NEXT: vmovdqa %ymm1, 64(%rdi)
; CHECK-NEXT: vmovdqa %ymm3, 96(%rdi)
; CHECK-NEXT: vmovdqa %ymm2, 32(%rdi)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
 %a = sext <16 x i8> %x to <16 x i64>
 store <16 x i64> %a, <16 x i64>* %y
 ret void
}

define dso_local void @vselect_split_v8i16_setcc(<8 x i16> %s, <8 x i16> %t, <8 x i64>* %p, <8 x i64>* %q, <8 x i64>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i16_setcc:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa (%rsi), %ymm2
; CHECK-NEXT: vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT: vpcmpeqw %xmm1, %xmm0, %k1
; CHECK-NEXT: kshiftrb $4, %k1, %k2
; CHECK-NEXT: vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT: vmovdqa64 (%rdi), %ymm2 {%k1}

```
; CHECK-NEXT:    vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:    vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %x = load <8 x i64>, <8 x i64>* %p
 %y = load <8 x i64>, <8 x i64>* %q
 %a = icmp eq <8 x i16> %s, %t
 %b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
 store <8 x i64> %b, <8 x i64>* %r
 ret void
}

define dso_local void @vselect_split_v8i32_setcc(<8 x i32> %s, <8 x i32> %t, <8 x i64>* %p, <8 x i64>* %q, <8
x i64>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v8i32_setcc:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rsi), %ymm2
; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:    vpcmpeqd %ymm1, %ymm0, %k1
; CHECK-NEXT:    kshiftrb $4, %k1, %k2
; CHECK-NEXT:    vmovdqa64 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT:    vmovdqa64 (%rdi), %ymm2 {%k1}
; CHECK-NEXT:    vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:    vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %x = load <8 x i64>, <8 x i64>* %p
 %y = load <8 x i64>, <8 x i64>* %q
 %a = icmp eq <8 x i32> %s, %t
 %b = select <8 x i1> %a, <8 x i64> %x, <8 x i64> %y
 store <8 x i64> %b, <8 x i64>* %r
 ret void
}

define dso_local void @vselect_split_v16i8_setcc(<16 x i8> %s, <16 x i8> %t, <16 x i32>* %p, <16 x i32>* %q,
<16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i8_setcc:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rsi), %ymm2
; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:    vpcmpeqb %xmm1, %xmm0, %k1
; CHECK-NEXT:    kshiftrw $8, %k1, %k2
; CHECK-NEXT:    vmovdqa32 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT:    vmovdqa32 (%rdi), %ymm2 {%k1}
; CHECK-NEXT:    vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:    vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
```

```
  %x = load <16 x i32>, <16 x i32>* %p
  %y = load <16 x i32>, <16 x i32>* %q
  %a = icmp eq <16 x i8> %s, %t
  %b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
  store <16 x i32> %b, <16 x i32>* %r
  ret void
}

define dso_local void @vselect_split_v16i16_setcc(<16 x i16> %s, <16 x i16> %t, <16 x i32>* %p, <16 x i32>*
%q, <16 x i32>* %r) "min-legal-vector-width"="256" {
; CHECK-LABEL: vselect_split_v16i16_setcc:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rsi), %ymm2
; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:    vpcmpeqw %ymm1, %ymm0, %k1
; CHECK-NEXT:    kshiftrw $8, %k1, %k2
; CHECK-NEXT:    vmovdqa32 32(%rdi), %ymm3 {%k2}
; CHECK-NEXT:    vmovdqa32 (%rdi), %ymm2 {%k1}
; CHECK-NEXT:    vmovdqa %ymm2, (%rdx)
; CHECK-NEXT:    vmovdqa %ymm3, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %x = load <16 x i32>, <16 x i32>* %p
  %y = load <16 x i32>, <16 x i32>* %q
  %a = icmp eq <16 x i16> %s, %t
  %b = select <16 x i1> %a, <16 x i32> %x, <16 x i32> %y
  store <16 x i32> %b, <16 x i32>* %r
  ret void
}

define <16 x i8> @trunc_packus_v16i32_v16i8(<16 x i32>* %p) "min-legal-vector-width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT:    vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT:    vpmovuswb %ymm0, %xmm0
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %a = load <16 x i32>, <16 x i32>* %p
  %b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32
255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
  %c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32
255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
  %d = icmp sgt <16 x i32> %c, zeroinitializer
  %e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer
  %f = trunc <16 x i32> %e to <16 x i8>
  ret <16 x i8> %f
```

```
}

define dso_local void @trunc_packus_v16i32_v16i8_store(<16 x i32>* %p, <16 x i8>* %q) "min-legal-vector-
width"="256" {
; CHECK-LABEL: trunc_packus_v16i32_v16i8_store:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vpackusdw 32(%rdi), %ymm0, %ymm0
; CHECK-NEXT:    vpermq {{.*#+}} ymm0 = ymm0[0,2,1,3]
; CHECK-NEXT:    vpmovuswb %ymm0, (%rsi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %a = load <16 x i32>, <16 x i32>* %p
 %b = icmp slt <16 x i32> %a, <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32
255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
 %c = select <16 x i1> %b, <16 x i32> %a, <16 x i32> <i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32
255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255, i32 255>
 %d = icmp sgt <16 x i32> %c, zeroinitializer
 %e = select <16 x i1> %d, <16 x i32> %c, <16 x i32> zeroinitializer
 %f = trunc <16 x i32> %e to <16 x i8>
 store <16 x i8> %f, <16 x i8>* %q
 ret void
}

define <64 x i1> @v64i1_argument_return(<64 x i1> %x) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_argument_return:
; CHECK:       # %bb.0:
; CHECK-NEXT:    retq
 ret <64 x i1> %x
}

define dso_local void @v64i1_shuffle(<64 x i8>* %x, <64 x i8>* %y) "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_shuffle:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    vmovdqa (%rdi), %ymm1
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm0
; CHECK-NEXT:    vptestnmb %ymm1, %ymm1, %k0
; CHECK-NEXT:    kshiftrd $1, %k0, %k1
; CHECK-NEXT:    movq $-3, %rax
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftlq $63, %k0, %k2
; CHECK-NEXT:    kshiftrq $62, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-5, %rax
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $3, %k0, %k2
```

```
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $61, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-9, %rax
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $2, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $60, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-17, %rax
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $5, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $59, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-33, %rax
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $4, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $58, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-65, %rax
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $7, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $57, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-129, %rax
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $6, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $56, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-257, %rax # imm = 0xFEFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $9, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $55, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-513, %rax # imm = 0xFDFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
```

```
; CHECK-NEXT:    kshiftrd $8, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $54, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-1025, %rax # imm = 0xFBFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $11, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $53, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-2049, %rax # imm = 0xF7FF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $10, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $52, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-4097, %rax # imm = 0xEFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $13, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $51, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-8193, %rax # imm = 0xDFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $12, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $50, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-16385, %rax # imm = 0xBFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $15, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $49, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-32769, %rax # imm = 0xFFFF7FFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $14, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $48, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-65537, %rax # imm = 0xFFFEFFFF
; CHECK-NEXT:    kmovq %rax, %k2
```

```
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $17, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $47, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-131073, %rax # imm = 0xFFFDFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $16, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $46, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-262145, %rax # imm = 0xFFFBFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $19, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $45, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-524289, %rax # imm = 0xFFF7FFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $18, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $44, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-1048577, %rax # imm = 0xFFEFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $21, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $43, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-2097153, %rax # imm = 0xFFDFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $20, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $42, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-4194305, %rax # imm = 0xFFBFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $23, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $41, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-8388609, %rax # imm = 0xFF7FFFFF
```

```
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $22, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $40, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-16777217, %rax # imm = 0xFEFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $25, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $39, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-33554433, %rax # imm = 0xFDFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $24, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $38, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-67108865, %rax # imm = 0xFBFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $27, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $37, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-134217729, %rax # imm = 0xF7FFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $26, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $36, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-268435457, %rax # imm = 0xEFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $29, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $35, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movq $-536870913, %rax # imm = 0xDFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $28, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $34, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
```

```
; CHECK-NEXT:    movq $-1073741825, %rax # imm = 0xBFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k1
; CHECK-NEXT:    kshiftrd $31, %k0, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $33, %k2, %k2
; CHECK-NEXT:    korq %k2, %k1, %k1
; CHECK-NEXT:    movabsq $-2147483649, %rax # imm = 0xFFFFFFFF7FFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k1, %k2
; CHECK-NEXT:    vptestnmb %ymm0, %ymm0, %k1
; CHECK-NEXT:    kshiftrd $30, %k0, %k0
; CHECK-NEXT:    kshiftlq $63, %k0, %k0
; CHECK-NEXT:    kshiftrq $32, %k0, %k0
; CHECK-NEXT:    korq %k0, %k2, %k0
; CHECK-NEXT:    movabsq $-4294967297, %rax # imm = 0xFFFFFFFEFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $1, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $31, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-8589934593, %rax # imm = 0xFFFFFFFDFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftlq $63, %k1, %k2
; CHECK-NEXT:    kshiftrq $30, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-17179869185, %rax # imm = 0xFFFFFFFBFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $3, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $29, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-34359738369, %rax # imm = 0xFFFFFFF7FFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $2, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $28, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-68719476737, %rax # imm = 0xFFFFFFEFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $5, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $27, %k2, %k2
```

```
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-137438953473, %rax # imm = 0xFFFFFFDFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $4, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $26, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-274877906945, %rax # imm = 0xFFFFFFBFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $7, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $25, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-549755813889, %rax # imm = 0xFFFFFF7FFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $6, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $24, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-1099511627777, %rax # imm = 0xFFFFFEFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $9, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $23, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-2199023255553, %rax # imm = 0xFFFFFDFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $8, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $22, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-4398046511105, %rax # imm = 0xFFFFFBFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $11, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $21, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-8796093022209, %rax # imm = 0xFFFFF7FFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $10, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
```

```
; CHECK-NEXT:    kshiftrq $20, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-17592186044417, %rax # imm = 0xFFFFEFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $13, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $19, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-35184372088833, %rax # imm = 0xFFFFDFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $12, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $18, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-70368744177665, %rax # imm = 0xFFFFBFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $15, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $17, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-140737488355329, %rax # imm = 0xFFFF7FFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $14, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $16, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-281474976710657, %rax # imm = 0xFFFEFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $17, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $15, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-562949953421313, %rax # imm = 0xFFFDFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $16, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $14, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-1125899906842625, %rax # imm = 0xFFFBFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $19, %k1, %k2
```

```
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $13, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-2251799813685249, %rax # imm = 0xFFF7FFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $18, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $12, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-4503599627370497, %rax # imm = 0xFFEFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $21, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $11, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-9007199254740993, %rax # imm = 0xFFDFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $20, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $10, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-18014398509481985, %rax # imm = 0xFFBFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $23, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $9, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-36028797018963969, %rax # imm = 0xFF7FFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $22, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $8, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-72057594037927937, %rax # imm = 0xFEFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $25, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $7, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-144115188075855873, %rax # imm = 0xFDFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
```

```
; CHECK-NEXT:    kshiftrd $24, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $6, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-288230376151711745, %rax # imm = 0xFBFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $27, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $5, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-576460752303423489, %rax # imm = 0xF7FFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $26, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $4, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-1152921504606846977, %rax # imm = 0xEFFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $29, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $3, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-2305843009213693953, %rax # imm = 0xDFFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $28, %k1, %k2
; CHECK-NEXT:    kshiftlq $63, %k2, %k2
; CHECK-NEXT:    kshiftrq $2, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    movabsq $-4611686018427387905, %rax # imm = 0xBFFFFFFFFFFFFFFF
; CHECK-NEXT:    kmovq %rax, %k2
; CHECK-NEXT:    kandq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $31, %k1, %k2
; CHECK-NEXT:    kshiftlq $62, %k2, %k2
; CHECK-NEXT:    korq %k2, %k0, %k0
; CHECK-NEXT:    kshiftrd $30, %k1, %k1
; CHECK-NEXT:    kshiftlq $1, %k0, %k0
; CHECK-NEXT:    kshiftrq $1, %k0, %k0
; CHECK-NEXT:    kshiftlq $63, %k1, %k1
; CHECK-NEXT:    korq %k1, %k0, %k1
; CHECK-NEXT:    vmovdqu8 %ymm1, (%rsi) {%k1}
; CHECK-NEXT:    kshiftrq $32, %k1, %k1
; CHECK-NEXT:    vmovdqu8 %ymm0, 32(%rsi) {%k1}
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
```

```
entry:
 %a = load <64 x i8>, <64 x i8>* %x
 %b = icmp eq <64 x i8> %a, zeroinitializer
 %shuf = shufflevector <64 x i1> %b, <64 x i1> undef, <64 x i32> <i32 1, i32 0, i32 3, i32 2, i32 5, i32 4, i32 7, i32
6, i32 9, i32 8, i32 11, i32 10, i32 13, i32 12, i32 15, i32 14, i32 17, i32 16, i32 19, i32 18, i32 21, i32 20, i32 23, i32
22, i32 25, i32 24, i32 27, i32 26, i32 29, i32 28, i32 31, i32 30, i32 33, i32 32, i32 35, i32 34, i32 37, i32 36, i32 39,
i32 38, i32 41, i32 40, i32 43, i32 42, i32 45, i32 44, i32 47, i32 46, i32 49, i32 48, i32 51, i32 50, i32 53, i32 52, i32
55, i32 54, i32 57, i32 56, i32 59, i32 58, i32 61, i32 60, i32 63, i32 62>
 call void @llvm.masked.store.v64i8.p0v64i8(<64 x i8> %a, <64 x i8>* %y, i32 1, <64 x i1> %shuf)
 ret void
}
declare void @llvm.masked.store.v64i8.p0v64i8(<64 x i8>, <64 x i8>*, i32, <64 x i1>)


@mem64_dst = dso_local global i64 0, align 8
@mem64_src = dso_local global i64 0, align 8
define dso_local i32 @v64i1_inline_asm() "min-legal-vector-width"="256" {
; CHECK-LABEL: v64i1_inline_asm:
; CHECK:       # %bb.0:
; CHECK-NEXT:    kmovq mem64_src(%rip), %k0
; CHECK-NEXT:    #APP
; CHECK-NEXT:    #NO_APP
; CHECK-NEXT:    kmovq %k0, mem64_dst(%rip)
; CHECK-NEXT:    movl -{{[0-9]+}}(%rsp), %eax
; CHECK-NEXT:    retq
 %1 = alloca i32, align 4
 %2 = load i64, i64* @mem64_src, align 8
 %3 = call i64 asm "", "=k,k,~{dirflag},~{fpsr},~{flags}"(i64 %2)
 store i64 %3, i64* @mem64_dst, align 8
 %4 = load i32, i32* %1, align 4
 ret i32 %4
}


define dso_local void @cmp_v8i64_sext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-
vector-width"="256" {
; CHECK-LABEL: cmp_v8i64_sext:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rsi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT:    vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT:    vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT:    vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:    vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %x = load <8 x i64>, <8 x i64>* %xptr
 %y = load <8 x i64>, <8 x i64>* %yptr
 %cmp = icmp slt <8 x i64> %x, %y
 %ext = sext <8 x i1> %cmp to <8 x i64>
```

```
  store <8 x i64> %ext, <8 x i64>* %zptr
  ret void
}


define dso_local void @cmp_v8i64_zext(<8 x i64>* %xptr, <8 x i64>* %yptr, <8 x i64>* %zptr) "min-legal-
vector-width"="256" {
; CHECK-LABEL: cmp_v8i64_zext:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rsi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT:    vpcmpgtq 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT:    vpcmpgtq (%rdi), %ymm0, %ymm0
; CHECK-NEXT:    vpsrlq $63, %ymm1, %ymm1
; CHECK-NEXT:    vpsrlq $63, %ymm0, %ymm0
; CHECK-NEXT:    vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:    vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %x = load <8 x i64>, <8 x i64>* %xptr
  %y = load <8 x i64>, <8 x i64>* %yptr
  %cmp = icmp slt <8 x i64> %x, %y
  %ext = zext <8 x i1> %cmp to <8 x i64>
  store <8 x i64> %ext, <8 x i64>* %zptr
  ret void
}


define <16 x i8> @var_rotate_v16i8(<16 x i8> %a, <16 x i8> %b) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: var_rotate_v16i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa {{.*#+}} xmm2 = [8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,8]
; CHECK-NEXT:    vpsubb %xmm1, %xmm2, %xmm2
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm1 =
xmm1[0],zero,xmm1[1],zero,xmm1[2],zero,xmm1[3],zero,xmm1[4],zero,xmm1[5],zero,xmm1[6],zero,xmm1[7],zer
o,xmm1[8],zero,xmm1[9],zero,xmm1[10],zero,xmm1[11],zero,xmm1[12],zero,xmm1[13],zero,xmm1[14],zero,xm
m1[15],zero
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm0 =
xmm0[0],zero,xmm0[1],zero,xmm0[2],zero,xmm0[3],zero,xmm0[4],zero,xmm0[5],zero,xmm0[6],zero,xmm0[7],zer
o,xmm0[8],zero,xmm0[9],zero,xmm0[10],zero,xmm0[11],zero,xmm0[12],zero,xmm0[13],zero,xmm0[14],zero,xm
m0[15],zero
; CHECK-NEXT:    vpsllvw %ymm1, %ymm0, %ymm1
; CHECK-NEXT:    vpmovzxbw {{.*#+}} ymm2 =
xmm2[0],zero,xmm2[1],zero,xmm2[2],zero,xmm2[3],zero,xmm2[4],zero,xmm2[5],zero,xmm2[6],zero,xmm2[7],zer
o,xmm2[8],zero,xmm2[9],zero,xmm2[10],zero,xmm2[11],zero,xmm2[12],zero,xmm2[13],zero,xmm2[14],zero,xm
m2[15],zero
; CHECK-NEXT:    vpsrlvw %ymm2, %ymm0, %ymm0
; CHECK-NEXT:    vpor %ymm0, %ymm1, %ymm0
; CHECK-NEXT:    vpmovwb %ymm0, %xmm0
; CHECK-NEXT:    vzeroupper
```

```
; CHECK-NEXT:    retq
%b8 = sub <16 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %b
%shl = shl <16 x i8> %a, %b
%lshr = lshr <16 x i8> %a, %b8
%or = or <16 x i8> %shl, %lshr
ret <16 x i8> %or
}


define <32 x i8> @var_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: var_rotate_v32i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpsllw $4, %ymm0, %ymm2
; CHECK-NEXT:    vpsrlw $4, %ymm0, %ymm3
; CHECK-NEXT:    vpternlogq $216, {{\.?LCPI[0-9]+_[0-9]+}}(%rip){1to4}, %ymm2, %ymm3
; CHECK-NEXT:    vpsllw $5, %ymm1, %ymm1
; CHECK-NEXT:    vpblendvb %ymm1, %ymm3, %ymm0, %ymm0
; CHECK-NEXT:    vpsllw $2, %ymm0, %ymm2
; CHECK-NEXT:    vpsrlw $6, %ymm0, %ymm3
; CHECK-NEXT:    vpternlogq $216, {{\.?LCPI[0-9]+_[0-9]+}}(%rip){1to4}, %ymm2, %ymm3
; CHECK-NEXT:    vpaddb %ymm1, %ymm1, %ymm1
; CHECK-NEXT:    vpblendvb %ymm1, %ymm3, %ymm0, %ymm0
; CHECK-NEXT:    vpsrlw $7, %ymm0, %ymm2
; CHECK-NEXT:    vpaddb %ymm0, %ymm0, %ymm3
; CHECK-NEXT:    vpternlogq $248, {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm2, %ymm3
; CHECK-NEXT:    vpaddb %ymm1, %ymm1, %ymm1
; CHECK-NEXT:    vpblendvb %ymm1, %ymm3, %ymm0, %ymm0
; CHECK-NEXT:    retq
%b8 = sub <32 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8
8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %b
%shl = shl <32 x i8> %a, %b
%lshr = lshr <32 x i8> %a, %b8
%or = or <32 x i8> %shl, %lshr
ret <32 x i8> %or
}


define <32 x i8> @splatvar_rotate_v32i8(<32 x i8> %a, <32 x i8> %b) nounwind "min-legal-vector-width"="256"
{
; CHECK-AVX512-LABEL: splatvar_rotate_v32i8:
; CHECK-AVX512:       # %bb.0:
; CHECK-AVX512-NEXT:    vpand {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm1, %xmm1
; CHECK-AVX512-NEXT:    vpmovzxbq {{.*#+}} xmm2 =
xmm1[0],zero,zero,zero,zero,zero,zero,zero,xmm1[1],zero,zero,zero,zero,zero,zero,zero
; CHECK-AVX512-NEXT:    vpsllw %xmm2, %ymm0, %ymm3
; CHECK-AVX512-NEXT:    vmovdqa {{.*#+}} xmm4 = [8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,8]
; CHECK-AVX512-NEXT:    vpsubb %xmm1, %xmm4, %xmm1
; CHECK-AVX512-NEXT:    vpcmpeqd %xmm4, %xmm4, %xmm4
; CHECK-AVX512-NEXT:    vpsllw %xmm2, %xmm4, %xmm2
; CHECK-AVX512-NEXT:    vpbroadcastb %xmm2, %ymm2
```

```
; CHECK-AVX512-NEXT:    vpmovzxbq {{.*#+}} xmm1 =
xmm1[0],zero,zero,zero,zero,zero,zero,zero,xmm1[1],zero,zero,zero,zero,zero,zero,zero
; CHECK-AVX512-NEXT:    vpsrlw %xmm1, %ymm0, %ymm5
; CHECK-AVX512-NEXT:    vpand %ymm2, %ymm3, %ymm2
; CHECK-AVX512-NEXT:    vpsrlw %xmm1, %xmm4, %xmm0
; CHECK-AVX512-NEXT:    vpsrlw $8, %xmm0, %xmm0
; CHECK-AVX512-NEXT:    vpbroadcastb %xmm0, %ymm0
; CHECK-AVX512-NEXT:    vpternlogq $236, %ymm5, %ymm2, %ymm0
; CHECK-AVX512-NEXT:    retq
;
; CHECK-VBMI-LABEL: splatvar_rotate_v32i8:
; CHECK-VBMI:       # %bb.0:
; CHECK-VBMI-NEXT:    vpand {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %xmm1, %xmm1
; CHECK-VBMI-NEXT:    vpmovzxbq {{.*#+}} xmm2 =
xmm1[0],zero,zero,zero,zero,zero,zero,zero,xmm1[1],zero,zero,zero,zero,zero,zero,zero
; CHECK-VBMI-NEXT:    vpsllw %xmm2, %ymm0, %ymm3
; CHECK-VBMI-NEXT:    vpcmpeqd %xmm4, %xmm4, %xmm4
; CHECK-VBMI-NEXT:    vpsllw %xmm2, %xmm4, %xmm2
; CHECK-VBMI-NEXT:    vpbroadcastb %xmm2, %ymm2
; CHECK-VBMI-NEXT:    vpand %ymm2, %ymm3, %ymm2
; CHECK-VBMI-NEXT:    vmovdqa {{.*#+}} xmm3 = [8,8,8,8,8,8,8,8,8,8,8,8,8,8,8,8]
; CHECK-VBMI-NEXT:    vpsubb %xmm1, %xmm3, %xmm1
; CHECK-VBMI-NEXT:    vpmovzxbq {{.*#+}} xmm1 =
xmm1[0],zero,zero,zero,zero,zero,zero,zero,xmm1[1],zero,zero,zero,zero,zero,zero,zero
; CHECK-VBMI-NEXT:    vpsrlw %xmm1, %ymm0, %ymm3
; CHECK-VBMI-NEXT:    vpsrlw %xmm1, %xmm4, %xmm0
; CHECK-VBMI-NEXT:    vmovdqa {{.*#+}} ymm1 =
[1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1]
; CHECK-VBMI-NEXT:    vpermb %ymm0, %ymm1, %ymm0
; CHECK-VBMI-NEXT:    vpternlogq $236, %ymm3, %ymm2, %ymm0
; CHECK-VBMI-NEXT:    retq
  %splat = shufflevector <32 x i8> %b, <32 x i8> undef, <32 x i32> zeroinitializer
  %splat8 = sub <32 x i8> <i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8
8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8, i8 8>, %splat
  %shl = shl <32 x i8> %a, %splat
  %lshr = lshr <32 x i8> %a, %splat8
  %or = or <32 x i8> %shl, %lshr
  ret <32 x i8> %or
}

define <32 x i8> @constant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
; CHECK-AVX512-LABEL: constant_rotate_v32i8:
; CHECK-AVX512:       # %bb.0:
; CHECK-AVX512-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-AVX512-NEXT:    vpunpckhbw {{.*#+}} ymm2 =
ymm0[8],ymm1[8],ymm0[9],ymm1[9],ymm0[10],ymm1[10],ymm0[11],ymm1[11],ymm0[12],ymm1[12],ymm0[13
],ymm1[13],ymm0[14],ymm1[14],ymm0[15],ymm1[15],ymm0[24],ymm1[24],ymm0[25],ymm1[25],ymm0[26],ym
m1[26],ymm0[27],ymm1[27],ymm0[28],ymm1[28],ymm0[29],ymm1[29],ymm0[30],ymm1[30],ymm0[31],ymm1[
```

31]

; CHECK-AVX512-NEXT: vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm2, %ymm2

; CHECK-AVX512-NEXT: vpsrlw $8, %ymm2, %ymm2

; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm1 =
ymm0[0],ymm1[0],ymm0[1],ymm1[1],ymm0[2],ymm1[2],ymm0[3],ymm1[3],ymm0[4],ymm1[4],ymm0[5],ymm1[5],ymm0[6],ymm1[6],ymm0[7],ymm1[7],ymm0[16],ymm1[16],ymm0[17],ymm1[17],ymm0[18],ymm1[18],ymm0[19],ymm1[19],ymm0[20],ymm1[20],ymm0[21],ymm1[21],ymm0[22],ymm1[22],ymm0[23],ymm1[23]

; CHECK-AVX512-NEXT: vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm1, %ymm1

; CHECK-AVX512-NEXT: vpsrlw $8, %ymm1, %ymm1

; CHECK-AVX512-NEXT: vpackuswb %ymm2, %ymm1, %ymm1

; CHECK-AVX512-NEXT: vpunpckhbw {{.*#+}} ymm2 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]

; CHECK-AVX512-NEXT: vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm2, %ymm2

; CHECK-AVX512-NEXT: vmovdqa {{.*#+}} ymm3 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255]

; CHECK-AVX512-NEXT: vpand %ymm3, %ymm2, %ymm2

; CHECK-AVX512-NEXT: vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]

; CHECK-AVX512-NEXT: vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm0, %ymm0

; CHECK-AVX512-NEXT: vpand %ymm3, %ymm0, %ymm0

; CHECK-AVX512-NEXT: vpackuswb %ymm2, %ymm0, %ymm0

; CHECK-AVX512-NEXT: vpor %ymm1, %ymm0, %ymm0

; CHECK-AVX512-NEXT: retq

;

; CHECK-VBMI-LABEL: constant_rotate_v32i8:

; CHECK-VBMI: # %bb.0:

; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm1 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]

; CHECK-VBMI-NEXT: vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm1, %ymm1

; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm2 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]

; CHECK-VBMI-NEXT: vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm2, %ymm2

; CHECK-VBMI-NEXT: vmovdqa {{.*#+}} ymm3 =
[0,2,4,6,8,10,12,14,32,34,36,38,40,42,44,46,16,18,20,22,24,26,28,30,48,50,52,54,56,58,60,62]

; CHECK-VBMI-NEXT: vpermi2b %ymm1, %ymm2, %ymm3

; CHECK-VBMI-NEXT: vpxor %xmm1, %xmm1, %xmm1

; CHECK-VBMI-NEXT: vpunpckhbw {{.*#+}} ymm2 =
ymm0[8],ymm1[8],ymm0[9],ymm1[9],ymm0[10],ymm1[10],ymm0[11],ymm1[11],ymm0[12],ymm1[12],ymm0[13],ymm1[13],ymm0[14],ymm1[14],ymm0[15],ymm1[15],ymm0[24],ymm1[24],ymm0[25],ymm1[25],ymm0[26],ymm1[26],ymm0[27],ymm1[27],ymm0[28],ymm1[28],ymm0[29],ymm1[29],ymm0[30],ymm1[30],ymm0[31],ymm1[31]

; CHECK-VBMI-NEXT: vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm2, %ymm2

; CHECK-VBMI-NEXT: vpsrlw $8, %ymm2, %ymm2

; CHECK-VBMI-NEXT: vpunpcklbw {{.*#+}} ymm0 =
ymm0[0],ymm1[0],ymm0[1],ymm1[1],ymm0[2],ymm1[2],ymm0[3],ymm1[3],ymm0[4],ymm1[4],ymm0[5],ymm1[5],ymm0[6],ymm1[6],ymm0[7],ymm1[7],ymm0[16],ymm1[16],ymm0[17],ymm1[17],ymm0[18],ymm1[18],ymm0[19],ymm1[19],ymm0[20],ymm1[20],ymm0[21],ymm1[21],ymm0[22],ymm1[22],ymm0[23],ymm1[23]

; CHECK-VBMI-NEXT: vpsllvw {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm0, %ymm0

```
; CHECK-VBMI-NEXT:    vpsrlw $8, %ymm0, %ymm0
; CHECK-VBMI-NEXT:    vpackuswb %ymm2, %ymm0, %ymm0
; CHECK-VBMI-NEXT:    vpor %ymm0, %ymm3, %ymm0
; CHECK-VBMI-NEXT:    retq
 %shl = shl <32 x i8> %a, <i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1, i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1>
 %lshr = lshr <32 x i8> %a, <i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1, i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7, i8 8, i8 7, i8 6, i8 5, i8 4, i8 3, i8 2, i8 1, i8 0, i8 1, i8 2, i8 3, i8 4, i8 5, i8 6, i8 7>
 %or = or <32 x i8> %shl, %lshr
 ret <32 x i8> %or
}


define <32 x i8> @splatconstant_rotate_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: splatconstant_rotate_v32i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpsllw $4, %ymm0, %ymm1
; CHECK-NEXT:    vpsrlw $4, %ymm0, %ymm0
; CHECK-NEXT:    vpternlogq $216, {{\.?LCPI[0-9]+_[0-9]+}}(%rip){1to4}, %ymm1, %ymm0
; CHECK-NEXT:    retq
 %shl = shl <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
 %lshr = lshr <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
 %or = or <32 x i8> %shl, %lshr
 ret <32 x i8> %or
}


define <32 x i8> @splatconstant_rotate_mask_v32i8(<32 x i8> %a) nounwind "min-legal-vector-width"="256" {
; CHECK-LABEL: splatconstant_rotate_mask_v32i8:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpsllw $4, %ymm0, %ymm1
; CHECK-NEXT:    vpsrlw $4, %ymm0, %ymm0
; CHECK-NEXT:    vpternlogq $216, {{\.?LCPI[0-9]+_[0-9]+}}(%rip){1to4}, %ymm1, %ymm0
; CHECK-NEXT:    vpand {{\.?LCPI[0-9]+_[0-9]+}}(%rip), %ymm0, %ymm0
; CHECK-NEXT:    retq
 %shl = shl <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
 %lshr = lshr <32 x i8> %a, <i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4, i8 4>
 %rmask = and <32 x i8> %lshr, <i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55, i8 55>
 %lmask = and <32 x i8> %shl, <i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33, i8 33>
 %or = or <32 x i8> %lmask, %rmask
 ret <32 x i8> %or
}
```

```
; RUN: llc -O3 -mtriple=powerpc-unknown-linux-gnu -mcpu=e500 -mattr=spe < %s | FileCheck %s

; PowerPC SPE is a rare in-tree target that has the FP_TO_SINT node marked
; as Legal.

; Verify that fptosi(42.1) isn't simplified when the rounding mode is
; unknown.
; Verify that no gross errors happen.
; CHECK-LABEL: @f20
; COMMON: cfdctsiz
define i32 @f20(double %a) strictfp {
entry:
 %result = call i32 @llvm.experimental.constrained.fptosi.i32.f64(double 42.1,
                               metadata !"fpexcept.strict")
                               strictfp
 ret i32 %result
}

@llvm.fp.env = thread_local global i8 zeroinitializer, section "llvm.metadata"
declare i32 @llvm.experimental.constrained.fptosi.i32.f64(double, metadata)
```
==

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```
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 output_name = "lldbPluginObjectContainerBSDArchive"
 configs += [ "//llvm/utils/gn/build:lldb_code" ]
 deps = [
   "//lldb/source/Core",
   "//lldb/source/Host",
   "//lldb/source/Symbol",
   "//llvm/lib/Support",
 ]
 sources = [ "ObjectContainerBSDArchive.cpp" ]
}
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1.112 clang 3.8.0

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```
; RUN: llc < %s -mtriple=s390x-linux-gnu -mcpu=zEC12 -verify-machineinstrs | FileCheck %s
;
; Test that early if conversion produces LOCR with operands of the right
; register classes.
```

```
define void @autogen_SD4739(i8*) {
; CHECK-NOT: Expected a GR32Bit register, but got a GRX32Bit register
BB:
 %L34 = load i8, i8* %0
 %Cmp56 = icmp sgt i8 undef, %L34
 br label %CF246

CF246:                                  ; preds = %CF246, %BB
 %Sl163 = select i1 %Cmp56, i8 %L34, i8 undef
 br i1 undef, label %CF246, label %CF248

CF248:                                  ; preds = %CF248, %CF246
 store i8 %Sl163, i8* %0
 br label %CF248
}
; NOTE: Assertions have been autogenerated by utils/update_llc_test_checks.py
; RUN: llc < %s -mtriple=x86_64-unknown-unknown -mattr=avx512vl,avx512bw,avx512dq,prefer-256-bit | FileCheck %s

; This file primarily contains tests for specific places in X86ISelLowering.cpp that needed be made aware of the legalizer not allowing 512-bit vectors due to prefer-256-bit even though AVX512 is enabled.

define void @add256(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="256" {
; CHECK-LABEL: add256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vpaddd (%rsi), %ymm0, %ymm0
; CHECK-NEXT:    vpaddd 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:    vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:    vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
 %d = load <16 x i32>, <16 x i32>* %a
 %e = load <16 x i32>, <16 x i32>* %b
 %f = add <16 x i32> %d, %e
 store <16 x i32> %f, <16 x i32>* %c
 ret void
}

define void @add512(<16 x i32>* %a, <16 x i32>* %b, <16 x i32>* %c) "min-legal-vector-width"="512" {
; CHECK-LABEL: add512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:    vpaddd (%rsi), %zmm0, %zmm0
; CHECK-NEXT:    vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
```

```llvm
  %d = load <16 x i32>, <16 x i32>* %a
  %e = load <16 x i32>, <16 x i32>* %b
  %f = add <16 x i32> %d, %e
  store <16 x i32> %f, <16 x i32>* %c
  ret void
}


define void @avg_v64i8_256(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="256" {
; CHECK-LABEL: avg_v64i8_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rsi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm1
; CHECK-NEXT:    vpavgb (%rdi), %ymm0, %ymm0
; CHECK-NEXT:    vpavgb 32(%rdi), %ymm1, %ymm1
; CHECK-NEXT:    vmovdqu %ymm1, (%rax)
; CHECK-NEXT:    vmovdqu %ymm0, (%rax)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %1 = load <64 x i8>, <64 x i8>* %a
  %2 = load <64 x i8>, <64 x i8>* %b
  %3 = zext <64 x i8> %1 to <64 x i32>
  %4 = zext <64 x i8> %2 to <64 x i32>
  %5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
  %6 = add nuw nsw <64 x i32> %5, %4
  %7 = lshr <64 x i32> %6, <i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32
1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1,
i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1, i32 1>
  %8 = trunc <64 x i32> %7 to <64 x i8>
  store <64 x i8> %8, <64 x i8>* undef, align 4
  ret void
}



define void @avg_v64i8_512(<64 x i8>* %a, <64 x i8>* %b) "min-legal-vector-width"="512" {
; CHECK-LABEL: avg_v64i8_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rsi), %zmm0
; CHECK-NEXT:    vpavgb (%rdi), %zmm0, %zmm0
; CHECK-NEXT:    vmovdqu64 %zmm0, (%rax)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %1 = load <64 x i8>, <64 x i8>* %a
  %2 = load <64 x i8>, <64 x i8>* %b
  %3 = zext <64 x i8> %1 to <64 x i32>
```

%4 = zext <64 x i8> %2 to <64 x i32>

%5 = add nuw nsw <64 x i32> %3, <i32 1, i32 1>

%6 = add nuw nsw <64 x i32> %5, %4

%7 = lshr <64 x i32> %6, <i32 1, i32 1>

%8 = trunc <64 x i32> %7 to <64 x i8>

store <64 x i8> %8, <64 x i8>* undef, align 4

ret void

}

define void @pmaddwd_32_256(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="256" {

; CHECK-LABEL: pmaddwd_32_256:

; CHECK: # %bb.0:

; CHECK-NEXT: vmovdqa (%rdi), %ymm0

; CHECK-NEXT: vmovdqa 32(%rdi), %ymm1

; CHECK-NEXT: vpmaddwd (%rsi), %ymm0, %ymm0

; CHECK-NEXT: vpmaddwd 32(%rsi), %ymm1, %ymm1

; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)

; CHECK-NEXT: vmovdqa %ymm0, (%rdx)

; CHECK-NEXT: vzeroupper

; CHECK-NEXT: retq

%A = load <32 x i16>, <32 x i16>* %APtr

%B = load <32 x i16>, <32 x i16>* %BPtr

%a = sext <32 x i16> %A to <32 x i32>

%b = sext <32 x i16> %B to <32 x i32>

%m = mul nsw <32 x i32> %a, %b

%odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32 12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>

%even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32 13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>

%ret = add <16 x i32> %odd, %even

store <16 x i32> %ret, <16 x i32>* %CPtr

ret void

}

define void @pmaddwd_32_512(<32 x i16>* %APtr, <32 x i16>* %BPtr, <16 x i32>* %CPtr) "min-legal-vector-width"="512" {

; CHECK-LABEL: pmaddwd_32_512:

; CHECK: # %bb.0:

; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0

; CHECK-NEXT: vpmaddwd (%rsi), %zmm0, %zmm0

; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)

```
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %A = load <32 x i16>, <32 x i16>* %APtr
  %B = load <32 x i16>, <32 x i16>* %BPtr
  %a = sext <32 x i16> %A to <32 x i32>
  %b = sext <32 x i16> %B to <32 x i32>
  %m = mul nsw <32 x i32> %a, %b
  %odd = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 0, i32 2, i32 4, i32 6, i32 8, i32 10, i32
12, i32 14, i32 16, i32 18, i32 20, i32 22, i32 24, i32 26, i32 28, i32 30>
  %even = shufflevector <32 x i32> %m, <32 x i32> undef, <16 x i32> <i32 1, i32 3, i32 5, i32 7, i32 9, i32 11, i32
13, i32 15, i32 17, i32 19, i32 21, i32 23, i32 25, i32 27, i32 29, i32 31>
  %ret = add <16 x i32> %odd, %even
  store <16 x i32> %ret, <16 x i32>* %CPtr
  ret void
}

define void @psubus_64i8_max_256(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-
width"="256" {
; CHECK-LABEL: psubus_64i8_max_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vpsubusb (%rsi), %ymm0, %ymm0
; CHECK-NEXT:    vpsubusb 32(%rsi), %ymm1, %ymm1
; CHECK-NEXT:    vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT:    vmovdqa %ymm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %x = load <64 x i8>, <64 x i8>* %xptr
  %y = load <64 x i8>, <64 x i8>* %yptr
  %cmp = icmp ult <64 x i8> %x, %y
  %max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
  %res = sub <64 x i8> %max, %y
  store <64 x i8> %res, <64 x i8>* %zptr
  ret void
}

define void @psubus_64i8_max_512(<64 x i8>* %xptr, <64 x i8>* %yptr, <64 x i8>* %zptr) "min-legal-vector-
width"="512" {
; CHECK-LABEL: psubus_64i8_max_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT:    vpsubusb (%rsi), %zmm0, %zmm0
; CHECK-NEXT:    vmovdqa64 %zmm0, (%rdx)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %x = load <64 x i8>, <64 x i8>* %xptr
  %y = load <64 x i8>, <64 x i8>* %yptr
```

```
%cmp = icmp ult <64 x i8> %x, %y
%max = select <64 x i1> %cmp, <64 x i8> %y, <64 x i8> %x
%res = sub <64 x i8> %max, %y
store <64 x i8> %res, <64 x i8>* %zptr
ret void
}


define i32 @_Z9test_charPcS_i_256(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-width"="256" {
; CHECK-LABEL: _Z9test_charPcS_i_256:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    movl %edx, %eax
; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:    xorl %ecx, %ecx
; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:    vpxor %xmm2, %xmm2, %xmm2
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB8_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %ymm3
; CHECK-NEXT:    vpmovsxbw 16(%rdi,%rcx), %ymm4
; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %ymm5
; CHECK-NEXT:    vpmaddwd %ymm3, %ymm5, %ymm3
; CHECK-NEXT:    vpaddd %ymm1, %ymm3, %ymm1
; CHECK-NEXT:    vpmovsxbw 16(%rsi,%rcx), %ymm3
; CHECK-NEXT:    vpmaddwd %ymm4, %ymm3, %ymm3
; CHECK-NEXT:    vpaddd %ymm2, %ymm3, %ymm2
; CHECK-NEXT:    addq $32, %rcx
; CHECK-NEXT:    cmpq %rcx, %rax
; CHECK-NEXT:    jne .LBB8_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm1
; CHECK-NEXT:    vpaddd %ymm0, %ymm2, %ymm0
; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:    vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vmovd %xmm0, %eax
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
entry:
  %3 = zext i32 %2 to i64
  br label %vector.body


vector.body:
```

```
%index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
%vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
%4 = getelementptr inbounds i8, i8* %0, i64 %index
%5 = bitcast i8* %4 to <32 x i8>*
%wide.load = load <32 x i8>, <32 x i8>* %5, align 1
%6 = sext <32 x i8> %wide.load to <32 x i32>
%7 = getelementptr inbounds i8, i8* %1, i64 %index
%8 = bitcast i8* %7 to <32 x i8>*
%wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
%9 = sext <32 x i8> %wide.load14 to <32 x i32>
%10 = mul nsw <32 x i32> %9, %6
%11 = add nsw <32 x i32> %10, %vec.phi
%index.next = add i64 %index, 32
%12 = icmp eq i64 %index.next, %3
br i1 %12, label %middle.block, label %vector.body


middle.block:
 %rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef>
 %bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
 %rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
 %rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
 %rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
 %rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
 %13 = extractelement <32 x i32> %bin.rdx20, i32 0
 ret i32 %13
}


define i32 @_Z9test_charPcS_i_512(i8* nocapture readonly, i8* nocapture readonly, i32) "min-legal-vector-
width"="512" {
```

```
; CHECK-LABEL: _Z9test_charPcS_i_512:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    movl %edx, %eax
; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:    xorl %ecx, %ecx
; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB9_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:    vpmovsxbw (%rdi,%rcx), %zmm2
; CHECK-NEXT:    vpmovsxbw (%rsi,%rcx), %zmm3
; CHECK-NEXT:    vpmaddwd %zmm2, %zmm3, %zmm2
; CHECK-NEXT:    vpaddd %zmm1, %zmm2, %zmm1
; CHECK-NEXT:    addq $32, %rcx
; CHECK-NEXT:    cmpq %rcx, %rax
; CHECK-NEXT:    jne .LBB9_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:    vpaddd %zmm0, %zmm1, %zmm0
; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vmovd %xmm0, %eax
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
entry:
 %3 = zext i32 %2 to i64
 br label %vector.body

vector.body:
 %index = phi i64 [ %index.next, %vector.body ], [ 0, %entry ]
 %vec.phi = phi <32 x i32> [ %11, %vector.body ], [ zeroinitializer, %entry ]
 %4 = getelementptr inbounds i8, i8* %0, i64 %index
 %5 = bitcast i8* %4 to <32 x i8>*
 %wide.load = load <32 x i8>, <32 x i8>* %5, align 1
 %6 = sext <32 x i8> %wide.load to <32 x i32>
 %7 = getelementptr inbounds i8, i8* %1, i64 %index
 %8 = bitcast i8* %7 to <32 x i8>*
 %wide.load14 = load <32 x i8>, <32 x i8>* %8, align 1
 %9 = sext <32 x i8> %wide.load14 to <32 x i32>
 %10 = mul nsw <32 x i32> %9, %6
 %11 = add nsw <32 x i32> %10, %vec.phi
 %index.next = add i64 %index, 32
 %12 = icmp eq i64 %index.next, %3
```

```llvm
  br i1 %12, label %middle.block, label %vector.body

middle.block:
  %rdx.shuf1 = shufflevector <32 x i32> %11, <32 x i32> undef, <32 x i32> <i32 16, i32 17, i32 18, i32 19, i32 20,
i32 21, i32 22, i32 23, i32 24, i32 25, i32 26, i32 27, i32 28, i32 29, i32 30, i32 31, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef>
  %bin.rdx1 = add <32 x i32> %11, %rdx.shuf1
  %rdx.shuf = shufflevector <32 x i32> %bin.rdx1, <32 x i32> undef, <32 x i32> <i32 8, i32 9, i32 10, i32 11, i32
12, i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx = add <32 x i32> %bin.rdx1, %rdx.shuf
  %rdx.shuf15 = shufflevector <32 x i32> %bin.rdx, <32 x i32> undef, <32 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx32 = add <32 x i32> %bin.rdx, %rdx.shuf15
  %rdx.shuf17 = shufflevector <32 x i32> %bin.rdx32, <32 x i32> undef, <32 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx18 = add <32 x i32> %bin.rdx32, %rdx.shuf17
  %rdx.shuf19 = shufflevector <32 x i32> %bin.rdx18, <32 x i32> undef, <32 x i32> <i32 1, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
  %bin.rdx20 = add <32 x i32> %bin.rdx18, %rdx.shuf19
  %13 = extractelement <32 x i32> %bin.rdx20, i32 0
  ret i32 %13
}

@a = global [1024 x i8] zeroinitializer, align 16
@b = global [1024 x i8] zeroinitializer, align 16

define i32 @sad_16i8_256() "min-legal-vector-width"="256" {
; CHECK-LABEL: sad_16i8_256:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:    movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT:    vpxor %xmm1, %xmm1, %xmm1
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB10_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:    vmovdqu a+1024(%rax), %xmm2
; CHECK-NEXT:    vpsadbw b+1024(%rax), %xmm2, %xmm2
; CHECK-NEXT:    vpaddd %ymm1, %ymm2, %ymm1
; CHECK-NEXT:    addq $4, %rax
```

```
; CHECK-NEXT:    jne .LBB10_1
; CHECK-NEXT: # %bb.2: # %middle.block
; CHECK-NEXT:    vpaddd %ymm0, %ymm1, %ymm0
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:    vpaddd %ymm1, %ymm0, %ymm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vmovd %xmm0, %eax
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
entry:
 br label %vector.body

vector.body:
 %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
 %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
 %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
 %1 = bitcast i8* %0 to <16 x i8>*
 %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
 %2 = zext <16 x i8> %wide.load to <16 x i32>
 %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
 %4 = bitcast i8* %3 to <16 x i8>*
 %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
 %5 = zext <16 x i8> %wide.load1 to <16 x i32>
 %6 = sub nsw <16 x i32> %2, %5
 %7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -
1, i32 -1, i32 -1, i32 -1, i32 -1>
 %8 = sub nsw <16 x i32> zeroinitializer, %6
 %9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
 %10 = add nsw <16 x i32> %9, %vec.phi
 %index.next = add i64 %index, 4
 %11 = icmp eq i64 %index.next, 1024
 br i1 %11, label %middle.block, label %vector.body

middle.block:
 %.lcssa = phi <16 x i32> [ %10, %vector.body ]
 %rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12,
i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
 %bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
 %rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef>
 %bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
 %rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
```

```
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}


define i32 @sad_16i8_512() "min-legal-vector-width"="512" {
; CHECK-LABEL: sad_16i8_512:
; CHECK:       # %bb.0: # %entry
; CHECK-NEXT:    vpxor %xmm0, %xmm0, %xmm0
; CHECK-NEXT:    movq $-1024, %rax # imm = 0xFC00
; CHECK-NEXT:    .p2align 4, 0x90
; CHECK-NEXT:  .LBB11_1: # %vector.body
; CHECK-NEXT:    # =>This Inner Loop Header: Depth=1
; CHECK-NEXT:    vmovdqu a+1024(%rax), %xmm1
; CHECK-NEXT:    vpsadbw b+1024(%rax), %xmm1, %xmm1
; CHECK-NEXT:    vpaddd %zmm0, %zmm1, %zmm0
; CHECK-NEXT:    addq $4, %rax
; CHECK-NEXT:    jne .LBB11_1
; CHECK-NEXT:  # %bb.2: # %middle.block
; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm1
; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm1
; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[2,3,0,1]
; CHECK-NEXT:    vpaddd %zmm1, %zmm0, %zmm0
; CHECK-NEXT:    vpshufd {{.*#+}} xmm1 = xmm0[1,1,2,3]
; CHECK-NEXT:    vpaddd %xmm1, %xmm0, %xmm0
; CHECK-NEXT:    vmovd %xmm0, %eax
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
entry:
  br label %vector.body

vector.body:
  %index = phi i64 [ 0, %entry ], [ %index.next, %vector.body ]
  %vec.phi = phi <16 x i32> [ zeroinitializer, %entry ], [ %10, %vector.body ]
  %0 = getelementptr inbounds [1024 x i8], [1024 x i8]* @a, i64 0, i64 %index
  %1 = bitcast i8* %0 to <16 x i8>*
  %wide.load = load <16 x i8>, <16 x i8>* %1, align 4
  %2 = zext <16 x i8> %wide.load to <16 x i32>
  %3 = getelementptr inbounds [1024 x i8], [1024 x i8]* @b, i64 0, i64 %index
  %4 = bitcast i8* %3 to <16 x i8>*
  %wide.load1 = load <16 x i8>, <16 x i8>* %4, align 4
  %5 = zext <16 x i8> %wide.load1 to <16 x i32>
```

```
%6 = sub nsw <16 x i32> %2, %5
%7 = icmp sgt <16 x i32> %6, <i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -1, i32 -
1, i32 -1, i32 -1, i32 -1, i32 -1>
%8 = sub nsw <16 x i32> zeroinitializer, %6
%9 = select <16 x i1> %7, <16 x i32> %6, <16 x i32> %8
%10 = add nsw <16 x i32> %9, %vec.phi
%index.next = add i64 %index, 4
%11 = icmp eq i64 %index.next, 1024
br i1 %11, label %middle.block, label %vector.body

middle.block:
%.lcssa = phi <16 x i32> [ %10, %vector.body ]
%rdx.shuf = shufflevector <16 x i32> %.lcssa, <16 x i32> undef, <16 x i32> <i32 8, i32 9, i32 10, i32 11, i32 12,
i32 13, i32 14, i32 15, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef>
%bin.rdx = add <16 x i32> %.lcssa, %rdx.shuf
%rdx.shuf2 = shufflevector <16 x i32> %bin.rdx, <16 x i32> undef, <16 x i32> <i32 4, i32 5, i32 6, i32 7, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef>
%bin.rdx2 = add <16 x i32> %bin.rdx, %rdx.shuf2
%rdx.shuf3 = shufflevector <16 x i32> %bin.rdx2, <16 x i32> undef, <16 x i32> <i32 2, i32 3, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
%bin.rdx3 = add <16 x i32> %bin.rdx2, %rdx.shuf3
%rdx.shuf4 = shufflevector <16 x i32> %bin.rdx3, <16 x i32> undef, <16 x i32> <i32 1, i32 undef, i32 undef, i32
undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef, i32 undef,
i32 undef, i32 undef>
%bin.rdx4 = add <16 x i32> %bin.rdx3, %rdx.shuf4
%12 = extractelement <16 x i32> %bin.rdx4, i32 0
ret i32 %12
}

define void @sbto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f32_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm1
; CHECK-NEXT:    vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT:    vmovaps %ymm1, (%rdi)
; CHECK-NEXT:    vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
%mask = icmp slt <16 x i16> %a, zeroinitializer
%1 = sitofp <16 x i1> %mask to <16 x float>
store <16 x float> %1, <16 x float>* %res
ret void
```

```
}

define void @sbto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f32_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = sitofp <16 x i1> %mask to <16 x float>
  store <16 x float> %1, <16 x float>* %res
  ret void
}

define void @sbto16f64_256(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="256" {
; CHECK-LABEL: sbto16f64_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT:    vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT:    vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT:    vmovaps %ymm3, (%rdi)
; CHECK-NEXT:    vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT:    vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = sitofp <16 x i1> %mask to <16 x double>
  store <16 x double> %1, <16 x double>* %res
  ret void
}

define void @sbto16f64_512(<16 x i16> %a, <16 x double>* %res)  "min-legal-vector-width"="512" {
; CHECK-LABEL: sbto16f64_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm1
```

```
; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:    vmovaps %zmm1, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = sitofp <16 x i1> %mask to <16 x double>
  store <16 x double> %1, <16 x double>* %res
  ret void
}


define void @ubto16f32_256(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f32_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT:    vcvtdq2ps %ymm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm1
; CHECK-NEXT:    vpsrld $31, %ymm1, %ymm1
; CHECK-NEXT:    vcvtdq2ps %ymm1, %ymm1
; CHECK-NEXT:    vmovaps %ymm1, (%rdi)
; CHECK-NEXT:    vmovaps %ymm0, 32(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = uitofp <16 x i1> %mask to <16 x float>
  store <16 x float> %1, <16 x float>* %res
  ret void
}


define void @ubto16f32_512(<16 x i16> %a, <16 x float>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f32_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT:    vcvtdq2ps %zmm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = uitofp <16 x i1> %mask to <16 x float>
  store <16 x float> %1, <16 x float>* %res
  ret void
}
```

```
define void @ubto16f64_256(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="256" {
; CHECK-LABEL: ubto16f64_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    kshiftrw $8, %k0, %k1
; CHECK-NEXT:    vpmovm2d %k1, %ymm0
; CHECK-NEXT:    vpsrld $31, %ymm0, %ymm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm1
; CHECK-NEXT:    vextracti128 $1, %ymm0, %xmm0
; CHECK-NEXT:    vcvtdq2pd %xmm0, %ymm0
; CHECK-NEXT:    vpmovm2d %k0, %ymm2
; CHECK-NEXT:    vpsrld $31, %ymm2, %ymm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm3
; CHECK-NEXT:    vextracti128 $1, %ymm2, %xmm2
; CHECK-NEXT:    vcvtdq2pd %xmm2, %ymm2
; CHECK-NEXT:    vmovaps %ymm2, 32(%rdi)
; CHECK-NEXT:    vmovaps %ymm3, (%rdi)
; CHECK-NEXT:    vmovaps %ymm0, 96(%rdi)
; CHECK-NEXT:    vmovaps %ymm1, 64(%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = uitofp <16 x i1> %mask to <16 x double>
  store <16 x double> %1, <16 x double>* %res
  ret void
}

define void @ubto16f64_512(<16 x i16> %a, <16 x double>* %res) "min-legal-vector-width"="512" {
; CHECK-LABEL: ubto16f64_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vpmovw2m %ymm0, %k0
; CHECK-NEXT:    vpmovm2d %k0, %zmm0
; CHECK-NEXT:    vpsrld $31, %zmm0, %zmm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm1
; CHECK-NEXT:    vextracti64x4 $1, %zmm0, %ymm0
; CHECK-NEXT:    vcvtdq2pd %ymm0, %zmm0
; CHECK-NEXT:    vmovaps %zmm0, 64(%rdi)
; CHECK-NEXT:    vmovaps %zmm1, (%rdi)
; CHECK-NEXT:    vzeroupper
; CHECK-NEXT:    retq
  %mask = icmp slt <16 x i16> %a, zeroinitializer
  %1 = uitofp <16 x i1> %mask to <16 x double>
  store <16 x double> %1, <16 x double>* %res
  ret void
}

define <16 x i16> @test_16f32toub_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
```

```
width"="256" {
; CHECK-LABEL: test_16f32toub_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:    vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:    vpmovd2m %ymm1, %k0
; CHECK-NEXT:    vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:    vpslld $31, %ymm1, %ymm1
; CHECK-NEXT:    vpmovd2m %ymm1, %k1
; CHECK-NEXT:    kunpckbw %k0, %k1, %k1
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:    retq
  %a = load <16 x float>, <16 x float>* %ptr
  %mask = fptoui <16 x float> %a to <16 x i1>
  %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
  ret <16 x i16> %select
}

define <16 x i16> @test_16f32toub_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {
; CHECK-LABEL: test_16f32toub_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:    vpslld $31, %zmm1, %zmm1
; CHECK-NEXT:    vpmovd2m %zmm1, %k1
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:    retq
  %a = load <16 x float>, <16 x float>* %ptr
  %mask = fptoui <16 x float> %a to <16 x i1>
  %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
  ret <16 x i16> %select
}

define <16 x i16> @test_16f32tosb_256(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="256" {
; CHECK-LABEL: test_16f32tosb_256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vcvttps2dq (%rdi), %ymm1
; CHECK-NEXT:    vpmovd2m %ymm1, %k0
; CHECK-NEXT:    vcvttps2dq 32(%rdi), %ymm1
; CHECK-NEXT:    vpmovd2m %ymm1, %k1
; CHECK-NEXT:    kunpckbw %k0, %k1, %k1
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:    retq
  %a = load <16 x float>, <16 x float>* %ptr
  %mask = fptosi <16 x float> %a to <16 x i1>
  %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
  ret <16 x i16> %select
```

```
}

define <16 x i16> @test_16f32tosb_512(<16 x float>* %ptr, <16 x i16> %passthru) "min-legal-vector-
width"="512" {
; CHECK-LABEL: test_16f32tosb_512:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vcvttps2dq (%rdi), %zmm1
; CHECK-NEXT:    vpmovd2m %zmm1, %k1
; CHECK-NEXT:    vmovdqu16 %ymm0, %ymm0 {%k1} {z}
; CHECK-NEXT:    retq
  %a = load <16 x float>, <16 x float>* %ptr
  %mask = fptosi <16 x float> %a to <16 x i1>
  %select = select <16 x i1> %mask, <16 x i16> %passthru, <16 x i16> zeroinitializer
  ret <16 x i16> %select
}

define void @mul256(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="256" {
; CHECK-LABEL: mul256:
; CHECK:       # %bb.0:
; CHECK-NEXT:    vmovdqa (%rdi), %ymm0
; CHECK-NEXT:    vmovdqa 32(%rdi), %ymm1
; CHECK-NEXT:    vmovdqa (%rsi), %ymm2
; CHECK-NEXT:    vmovdqa 32(%rsi), %ymm3
; CHECK-NEXT:    vpunpckhbw {{.*#+}} ymm4 =
ymm2[8],ymm0[8],ymm2[9],ymm0[9],ymm2[10],ymm0[10],ymm2[11],ymm0[11],ymm2[12],ymm0[12],ymm2[13
],ymm0[13],ymm2[14],ymm0[14],ymm2[15],ymm0[15],ymm2[24],ymm0[24],ymm2[25],ymm0[25],ymm2[26],ym
m0[26],ymm2[27],ymm0[27],ymm2[28],ymm0[28],ymm2[29],ymm0[29],ymm2[30],ymm0[30],ymm2[31],ymm0[
31]
; CHECK-NEXT:    vpunpckhbw {{.*#+}} ymm5 =
ymm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31]
; CHECK-NEXT:    vpmullw %ymm4, %ymm5, %ymm4
; CHECK-NEXT:    vmovdqa {{.*#+}} ymm5 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255]
; CHECK-NEXT:    vpand %ymm5, %ymm4, %ymm4
; CHECK-NEXT:    vpunpcklbw {{.*#+}} ymm2 =
ymm2[0],ymm0[0],ymm2[1],ymm0[1],ymm2[2],ymm0[2],ymm2[3],ymm0[3],ymm2[4],ymm0[4],ymm2[5],ymm0[
5],ymm2[6],ymm0[6],ymm2[7],ymm0[7],ymm2[16],ymm0[16],ymm2[17],ymm0[17],ymm2[18],ymm0[18],ymm2[
19],ymm0[19],ymm2[20],ymm0[20],ymm2[21],ymm0[21],ymm2[22],ymm0[22],ymm2[23],ymm0[23]
; CHECK-NEXT:    vpunpcklbw {{.*#+}} ymm0 =
ymm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23]
; CHECK-NEXT:    vpmullw %ymm2, %ymm0, %ymm0
; CHECK-NEXT:    vpand %ymm5, %ymm0, %ymm0
; CHECK-NEXT:    vpackuswb %ymm4, %ymm0, %ymm0
; CHECK-NEXT:    vpunpckhbw {{.*#+}} ymm2 =
ymm3[8],ymm0[8],ymm3[9],ymm0[9],ymm3[10],ymm0[10],ymm3[11],ymm0[11],ymm3[12],ymm0[12],ymm3[13
],ymm0[13],ymm3[14],ymm0[14],ymm3[15],ymm0[15],ymm3[24],ymm0[24],ymm3[25],ymm0[25],ymm3[26],ym
m0[26],ymm3[27],ymm0[27],ymm3[28],ymm0[28],ymm3[29],ymm0[29],ymm3[30],ymm0[30],ymm3[31],ymm0[
31]
```

; CHECK-NEXT: vpunpckhbw {{.*#+}} ymm4 =
ymm1[8],ymm0[8],ymm1[9],ymm0[9],ymm1[10],ymm0[10],ymm1[11],ymm0[11],ymm1[12],ymm0[12],ymm1[13
],ymm0[13],ymm1[14],ymm0[14],ymm1[15],ymm0[15],ymm1[24],ymm0[24],ymm1[25],ymm0[25],ymm1[26],ym
m0[26],ymm1[27],ymm0[27],ymm1[28],ymm0[28],ymm1[29],ymm0[29],ymm1[30],ymm0[30],ymm1[31],ymm0[
31]
; CHECK-NEXT: vpmullw %ymm2, %ymm4, %ymm2
; CHECK-NEXT: vpand %ymm5, %ymm2, %ymm2
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm3 =
ymm3[0],ymm0[0],ymm3[1],ymm0[1],ymm3[2],ymm0[2],ymm3[3],ymm0[3],ymm3[4],ymm0[4],ymm3[5],ymm0[
5],ymm3[6],ymm0[6],ymm3[7],ymm0[7],ymm3[16],ymm0[16],ymm3[17],ymm0[17],ymm3[18],ymm0[18],ymm3[
19],ymm0[19],ymm3[20],ymm0[20],ymm3[21],ymm0[21],ymm3[22],ymm0[22],ymm3[23],ymm0[23]
; CHECK-NEXT: vpunpcklbw {{.*#+}} ymm1 =
ymm1[0],ymm0[0],ymm1[1],ymm0[1],ymm1[2],ymm0[2],ymm1[3],ymm0[3],ymm1[4],ymm0[4],ymm1[5],ymm0[
5],ymm1[6],ymm0[6],ymm1[7],ymm0[7],ymm1[16],ymm0[16],ymm1[17],ymm0[17],ymm1[18],ymm0[18],ymm1[
19],ymm0[19],ymm1[20],ymm0[20],ymm1[21],ymm0[21],ymm1[22],ymm0[22],ymm1[23],ymm0[23]
; CHECK-NEXT: vpmullw %ymm3, %ymm1, %ymm1
; CHECK-NEXT: vpand %ymm5, %ymm1, %ymm1
; CHECK-NEXT: vpackuswb %ymm2, %ymm1, %ymm1
; CHECK-NEXT: vmovdqa %ymm1, 32(%rdx)
; CHECK-NEXT: vmovdqa %ymm0, (%rdx)
; CHECK-NEXT: vzeroupper
; CHECK-NEXT: retq
 %d = load <64 x i8>, <64 x i8>* %a
 %e = load <64 x i8>, <64 x i8>* %b
 %f = mul <64 x i8> %d, %e
 store <64 x i8> %f, <64 x i8>* %c
 ret void
}

define void @mul512(<64 x i8>* %a, <64 x i8>* %b, <64 x i8>* %c) "min-legal-vector-width"="512" {
; CHECK-LABEL: mul512:
; CHECK: # %bb.0:
; CHECK-NEXT: vmovdqa64 (%rdi), %zmm0
; CHECK-NEXT: vmovdqa64 (%rsi), %zmm1
; CHECK-NEXT: vpunpckhbw {{.*#+}} zmm2 =
zmm1[8],zmm0[8],zmm1[9],zmm0[9],zmm1[10],zmm0[10],zmm1[11],zmm0[11],zmm1[12],zmm0[12],zmm1[13],
zmm0[13],zmm1[14],zmm0[14],zmm1[15],zmm0[15],zmm1[24],zmm0[24],zmm1[25],zmm0[25],zmm1[26],zmm0
[26],zmm1[27],zmm0[27],zmm1[28],zmm0[28],zmm1[29],zmm0[29],zmm1[30],zmm0[30],zmm1[31],zmm0[31],z
mm1[40],zmm0[40],zmm1[41],zmm0[41],zmm1[42],zmm0[42],zmm1[43],zmm0[43],zmm1[44],zmm0[44],zmm1[
45],zmm0[45],zmm1[46],zmm0[46],zmm1[47],zmm0[47],zmm1[56],zmm0[56],zmm1[57],zmm0[57],zmm1[58],z
mm0[58],zmm1[59],zmm0[59],zmm1[60],zmm0[60],zmm1[61],zmm0[61],zmm1[62],zmm0[62],zmm1[63],zmm0[
63]
; CHECK-NEXT: vpunpckhbw {{.*#+}} zmm3 =
zmm0[8,8,9,9,10,10,11,11,12,12,13,13,14,14,15,15,24,24,25,25,26,26,27,27,28,28,29,29,30,30,31,31,40,40,41,41,4
2,42,43,43,44,44,45,45,46,46,47,47,56,56,57,57,58,58,59,59,60,60,61,61,62,62,63,63]
; CHECK-NEXT: vpmullw %zmm2, %zmm3, %zmm2
; CHECK-NEXT: vmovdqa64 {{.*#+}} zmm3 =
[255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,255,2

55,255,255,255,255,255]

; CHECK-NEXT: vpandq %zmm3, %zmm2, %zmm2

; CHECK-NEXT: vpunpcklbw {{.*#+}} zmm1 = zmm1[0],zmm0[0],zmm1[1],zmm0[1],zmm1[2],zmm0[2],zmm1[3],zmm0[3],zmm1[4],zmm0[4],zmm1[5],zmm0[5],zmm1[6],zmm0[6],zmm1[7],zmm0[7],zmm1[16],zmm0[16],zmm1[17],zmm0[17],zmm1[18],zmm0[18],zmm1[19],zmm0[19],zmm1[20],zmm0[20],zmm1[21],zmm0[21],zmm1[22],zmm0[22],zmm1[23],zmm0[23],zmm1[32],zmm0[32],zmm1[33],zmm0[33],zmm1[34],zmm0[34],zmm1[35],zmm0[35],zmm1[36],zmm0[36],zmm1[37],zmm0[37],zmm1[38],zmm0[38],zmm1[39],zmm0[39],zmm1[48],zmm0[48],zmm1[49],zmm0[49],zmm1[50],zmm0[50],zmm1[51],zmm0[51],zmm1[52],zmm0[52],zmm1[53],zmm0[53],zmm1[54],zmm0[54],zmm1[55],zmm0[55]

; CHECK-NEXT: vpunpcklbw {{.*#+}} zmm0 = zmm0[0,0,1,1,2,2,3,3,4,4,5,5,6,6,7,7,16,16,17,17,18,18,19,19,20,20,21,21,22,22,23,23,32,32,33,33,34,34,35,35,36,36,37,37,38,38,39,39,48,48,49,49,50,50,51,51,52,52,53,53,54,54,55,55]

; CHECK-NEXT: vpmullw %zmm1, %zmm0, %zmm0

; CHECK-NEXT: vpandq %zmm3, %zmm0, %zmm0

; CHECK-NEXT: vpackuswb %zmm2, %zmm0, %zmm0

; CHECK-NEXT: vmovdqa64 %zmm0, (%rdx)

; CHECK-NEXT: vzeroupper

; CHECK-NEXT: retq

 %d = load <64 x i8>, <64 x i8>* %a

 %e = load <64 x i8>, <64 x i8>* %b

 %f = mul <64 x i8> %d, %e

 store <64 x i8> %f, <64 x i8>* %c

 ret void

}

; NOTE: Assertions have been autogenerated by utils/update_analyze_test_checks.py
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx2 | FileCheck %s --check-prefixes=CHECK,VEC256,AVX
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,+prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC256,SKX256
; RUN: opt < %s -cost-model -analyze -mtriple=x86_64-apple-macosx10.8.0 -mattr=+avx512vl,+avx512bw,+avx512dq,-prefer-256-bit | FileCheck %s --check-prefixes=CHECK,VEC512

define void @zext256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'zext256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'zext256'
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
  %A = zext <8 x i16> undef to <8 x i64>
  %B = zext <8 x i32> undef to <8 x i64>
  %C = zext <16 x i8> undef to <16 x i32>
  %D = zext <16 x i16> undef to <16 x i32>
  %E = zext <32 x i8> undef to <32 x i16>
  ret void
}

define void @zext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'zext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = zext <8 x i16> undef to <8 x i64>

; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'zext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'zext512'
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %A = zext <8 x i16> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = zext <8 x i32> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = zext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = zext <16 x i16> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = zext <32 x i8> undef to <32 x i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
  %A = zext <8 x i16> undef to <8 x i64>
  %B = zext <8 x i32> undef to <8 x i64>
  %C = zext <16 x i8> undef to <16 x i32>
  %D = zext <16 x i16> undef to <16 x i32>
  %E = zext <32 x i8> undef to <32 x i16>
  ret void
}

define void @sext256() "min-legal-vector-width"="256" {
; VEC256-LABEL: 'sext256'
; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>

; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>

; VEC256-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; VEC256-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; VEC256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

; VEC512-LABEL: 'sext256'

; VEC512-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x i64>

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>

; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>

; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void

;

 %A = sext <8 x i8> undef to <8 x i64>
 %B = sext <8 x i16> undef to <8 x i64>
 %C = sext <8 x i32> undef to <8 x i64>
 %D = sext <16 x i8> undef to <16 x i32>
 %E = sext <16 x i16> undef to <16 x i32>
 %F = sext <32 x i8> undef to <32 x i16>
 ret void
}

define void @sext512() "min-legal-vector-width"="512" {
; AVX-LABEL: 'sext512'
; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 7 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 4 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; AVX-NEXT: Cost Model: Found an estimated cost of 3 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; AVX-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; SKX256-LABEL: 'sext512'
; SKX256-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>

; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x

i64>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; SKX256-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; SKX256-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
; VEC512-LABEL: 'sext512'
; VEC512-NEXT: Cost Model: Found an estimated cost of 24 for instruction: %A = sext <8 x i8> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %B = sext <8 x i16> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %C = sext <8 x i32> undef to <8 x i64>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %D = sext <16 x i8> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %E = sext <16 x i16> undef to <16 x i32>
; VEC512-NEXT: Cost Model: Found an estimated cost of 1 for instruction: %F = sext <32 x i8> undef to <32 x i16>
; VEC512-NEXT: Cost Model: Found an estimated cost of 0 for instruction: ret void
;
 %A = sext <8 x i8> undef to <8 x i64>
 %B = sext <8 x i16> undef to <8 x i64>
 %C = sext <8 x i32> undef to <8 x i64>
 %D = sext <16 x i8> undef to <16 x i32>
 %E = sext <16 x i16> undef to <16 x i32>
 %F = sext <32 x i8> undef to <32 x i16>
 ret void
}
$OpenBSD: COPYRIGHT,v 1.3 2003/06/02 20:18:36 millert Exp $

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=-=
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*/
; RUN: llc -march=hexagon < %s
; REQUIRES: asserts

; The two loads based on %struct.0, loading two different data types
; cause LSR to assume type "void" for the memory type. This would then
; cause an assert in isLegalAddressingMode. Make sure we no longer crash.

target triple = "hexagon"

%struct.0 = type { i8*, i8, %union.anon.0 }

```llvm
%union.anon.0 = type { i8* }

define hidden fastcc void @fred() unnamed_addr #0 {
entry:
 br i1 undef, label %while.end, label %while.body.lr.ph

while.body.lr.ph:                       ; preds = %entry
 br label %while.body

while.body:                             ; preds = %exit.2, %while.body.lr.ph
 %lsr.iv = phi %struct.0* [ %cgep22, %exit.2 ], [ undef, %while.body.lr.ph ]
 switch i32 undef, label %exit [
   i32 1, label %sw.bb.i
   i32 2, label %sw.bb3.i
 ]

sw.bb.i:                                ; preds = %while.body
 unreachable

sw.bb3.i:                               ; preds = %while.body
 unreachable

exit:                                   ; preds = %while.body
 switch i32 undef, label %exit.2 [
   i32 1, label %sw.bb.i17
   i32 2, label %sw.bb3.i20
 ]

sw.bb.i17:                              ; preds = %.exit
 %0 = bitcast %struct.0* %lsr.iv to i32*
 %1 = load i32, i32* %0, align 4
 unreachable

sw.bb3.i20:                             ; preds = %exit
 %2 = bitcast %struct.0* %lsr.iv to i8**
 %3 = load i8*, i8** %2, align 4
 unreachable

exit.2:                                 ; preds = %exit
 %cgep22 = getelementptr %struct.0, %struct.0* %lsr.iv, i32 1
 br label %while.body

while.end:                              ; preds = %entry
 ret void
}

attributes #0 = { nounwind optsize "target-cpu"="hexagonv55" }
```

```
; RUN: llc -mtriple=aarch64-apple-ios %s -o - | FileCheck %s

define <16 x double> @test_sitofp_fixed(<16 x i32> %in) {
; CHECK-LABEL: test_sitofp_fixed:

 ; First, extend each i32 to i64
; CHECK-DAG: sshll2.2d [[BLOCK0_HI:v[0-9]+]], v0, #0
; CHECK-DAG: sshll2.2d [[BLOCK1_HI:v[0-9]+]], v1, #0
; CHECK-DAG: sshll2.2d [[BLOCK2_HI:v[0-9]+]], v2, #0
; CHECK-DAG: sshll2.2d [[BLOCK3_HI:v[0-9]+]], v3, #0
; CHECK-DAG: sshll.2d [[BLOCK0_LO:v[0-9]+]], v0, #0
; CHECK-DAG: sshll.2d [[BLOCK1_LO:v[0-9]+]], v1, #0
; CHECK-DAG: sshll.2d [[BLOCK2_LO:v[0-9]+]], v2, #0
; CHECK-DAG: sshll.2d [[BLOCK3_LO:v[0-9]+]], v3, #0

 ; Next, convert each to double.
; CHECK-DAG: scvtf.2d v0, [[BLOCK0_LO]]
; CHECK-DAG: scvtf.2d v1, [[BLOCK0_HI]]
; CHECK-DAG: scvtf.2d v2, [[BLOCK1_LO]]
; CHECK-DAG: scvtf.2d v3, [[BLOCK1_HI]]
; CHECK-DAG: scvtf.2d v4, [[BLOCK2_LO]]
; CHECK-DAG: scvtf.2d v5, [[BLOCK2_HI]]
; CHECK-DAG: scvtf.2d v6, [[BLOCK3_LO]]
; CHECK-DAG: scvtf.2d v7, [[BLOCK3_HI]]

; CHECK: ret
 %flt = sitofp <16 x i32> %in to <16 x double>
 %res = fdiv <16 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0, double 64.0>
 ret <16 x double> %res
}

; This one is small enough to satisfy isSimple, but still illegally large.
define <4 x double> @test_sitofp_fixed_shortish(<4 x i64> %in) {
; CHECK-LABEL: test_sitofp_fixed_shortish:

; CHECK-DAG: scvtf.2d v0, v0
; CHECK-DAG: scvtf.2d v1, v1

; CHECK: ret
 %flt = sitofp <4 x i64> %in to <4 x double>
 %res = fdiv <4 x double> %flt, <double 64.0, double 64.0, double 64.0, double 64.0>
 ret <4 x double> %res
}
; RUN: opt %s -inline -S | FileCheck %s

define internal void @innerSmall() "min-legal-vector-width"="128" {
```

```
 ret void
}

define internal void @innerLarge() "min-legal-vector-width"="512" {
 ret void
}

define internal void @innerNoAttribute() {
 ret void
}

; We should not add an attribute during inlining. No attribute means unknown.
; Inlining doesn't change the fact that we don't know anything about this
; function.
define void @outerNoAttribute() {
 call void @innerLarge()
 ret void
}

define void @outerConflictingAttributeSmall() "min-legal-vector-width"="128" {
 call void @innerLarge()
 ret void
}

define void @outerConflictingAttributeLarge() "min-legal-vector-width"="512" {
 call void @innerSmall()
 ret void
}

; We should remove the attribute after inlining since the callee's
; vector width requirements are unknown.
define void @outerAttribute() "min-legal-vector-width"="128" {
 call void @innerNoAttribute()
 ret void
}

; CHECK: define void @outerNoAttribute() {
; CHECK: define void @outerConflictingAttributeSmall() #0
; CHECK: define void @outerConflictingAttributeLarge() #0
; CHECK: define void @outerAttribute() {
; CHECK: attributes #0 = { "min-legal-vector-width"="512" }
; RUN: opt -consthoist -S -o - %s | FileCheck %s
target datalayout = "e-m:e-p:32:32-i64:64-v128:64:128-a:0:32-n32-S64"
target triple = "thumbv6m-none--musleabi"

; Check that for i8 type, the maximum legal offset is 31.
; Also check that an constant used as value to be stored rather than
; pointer in a store instruction is hoisted.
```

```
; CHECK: foo_i8
; CHECK-DAG:  %[[C1:const[0-9]?]] = bitcast i32 805874720 to i32
; CHECK-DAG:  %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK-DAG:  %[[C3:const[0-9]?]] = bitcast i32 805873720 to i32
; CHECK-DAG:  %[[C4:const[0-9]?]] = bitcast i32 805873688 to i32
; CHECK:  %0 = inttoptr i32 %[[C2]] to i8*
; CHECK-NEXT:  %1 = load volatile i8, i8* %0
; CHECK-NEXT:  %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT:  %2 = inttoptr i32 %[[M1]] to i8*
; CHECK-NEXT:  %3 = load volatile i8, i8* %2
; CHECK-NEXT:  %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 31
; CHECK-NEXT:  %4 = inttoptr i32 %[[M2]] to i8*
; CHECK-NEXT:  %5 = load volatile i8, i8* %4
; CHECK-NEXT:  %6 = inttoptr i32 %[[C1]] to i8*
; CHECK-NEXT:  %7 = load volatile i8, i8* %6
; CHECK-NEXT:  %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 7
; CHECK-NEXT:  %8 = inttoptr i32 %[[M3]] to i8*
; CHECK-NEXT:  %9 = load volatile i8, i8* %8
; CHECK-NEXT:  %10 = inttoptr i32 %[[C4]] to i8*
; CHECK-NEXT:  store i8 %9, i8* %10
; CHECK-NEXT:  %[[M4:const_mat[0-9]?]] = add i32 %[[C4]], 31
; CHECK-NEXT:  %11 = inttoptr i32 %[[M4]] to i8*
; CHECK-NEXT:  store i8 %7, i8* %11
; CHECK-NEXT:  %12 = inttoptr i32 %[[C3]] to i8*
; CHECK-NEXT:  store i8 %5, i8* %12
; CHECK-NEXT:  %[[M5:const_mat[0-9]?]] = add i32 %[[C3]], 7
; CHECK-NEXT:  %13 = inttoptr i32 %[[M5]] to i8*
; CHECK-NEXT:  store i8 %3, i8* %13
; CHECK-NEXT:  %[[M6:const_mat[0-9]?]] = add i32 %[[C1]], 80
; CHECK-NEXT:  %14 = inttoptr i32 %[[M6]] to i8*
; CHECK-NEXT:  store i8* %14, i8** @goo

@goo = global i8* undef

define void @foo_i8() {
entry:
 %0 = load volatile i8, i8* inttoptr (i32 805874688 to i8*)
 %1 = load volatile i8, i8* inttoptr (i32 805874692 to i8*)
 %2 = load volatile i8, i8* inttoptr (i32 805874719 to i8*)
 %3 = load volatile i8, i8* inttoptr (i32 805874720 to i8*)
 %4 = load volatile i8, i8* inttoptr (i32 805874727 to i8*)
 store i8 %4, i8* inttoptr(i32 805873688 to i8*)
 store i8 %3, i8* inttoptr(i32 805873719 to i8*)
 store i8 %2, i8* inttoptr(i32 805873720 to i8*)
 store i8 %1, i8* inttoptr(i32 805873727 to i8*)
 store i8* inttoptr(i32 805874800 to i8*), i8** @goo
 ret void
}
```

; Check that for i16 type, the maximum legal offset is 62.
; CHECK: foo_i16
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874752 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i16*
; CHECK-NEXT: %1 = load volatile i16, i16* %0, align 2
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i16*
; CHECK-NEXT: %3 = load volatile i16, i16* %2, align 2
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 32
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i16*
; CHECK-NEXT: %5 = load volatile i16, i16* %4, align 2
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C2]], 62
; CHECK-NEXT: %6 = inttoptr i32 %[[M3]] to i16*
; CHECK-NEXT: %7 = load volatile i16, i16* %6, align 2
; CHECK-NEXT: %8 = inttoptr i32 %[[C1]] to i16*
; CHECK-NEXT: %9 = load volatile i16, i16* %8, align 2
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 22
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i16*
; CHECK-NEXT: %11 = load volatile i16, i16* %10, align 2

define void @foo_i16() {
entry:
 %0 = load volatile i16, i16* inttoptr (i32 805874688 to i16*), align 2
 %1 = load volatile i16, i16* inttoptr (i32 805874692 to i16*), align 2
 %2 = load volatile i16, i16* inttoptr (i32 805874720 to i16*), align 2
 %3 = load volatile i16, i16* inttoptr (i32 805874750 to i16*), align 2
 %4 = load volatile i16, i16* inttoptr (i32 805874752 to i16*), align 2
 %5 = load volatile i16, i16* inttoptr (i32 805874774 to i16*), align 2
 ret void
}

; Check that for i32 type, the maximum legal offset is 124.
; CHECK: foo_i32
; CHECK-DAG: %[[C1:const[0-9]?]] = bitcast i32 805874816 to i32
; CHECK-DAG: %[[C2:const[0-9]?]] = bitcast i32 805874688 to i32
; CHECK: %0 = inttoptr i32 %[[C2]] to i32*
; CHECK-NEXT: %1 = load volatile i32, i32* %0, align 4
; CHECK-NEXT: %[[M1:const_mat[0-9]?]] = add i32 %[[C2]], 4
; CHECK-NEXT: %2 = inttoptr i32 %[[M1]] to i32*
; CHECK-NEXT: %3 = load volatile i32, i32* %2, align 4
; CHECK-NEXT: %[[M2:const_mat[0-9]?]] = add i32 %[[C2]], 124
; CHECK-NEXT: %4 = inttoptr i32 %[[M2]] to i32*
; CHECK-NEXT: %5 = load volatile i32, i32* %4, align 4
; CHECK-NEXT: %6 = inttoptr i32 %[[C1]] to i32*
; CHECK-NEXT: %7 = load volatile i32, i32* %6, align 4
; CHECK-NEXT: %[[M3:const_mat[0-9]?]] = add i32 %[[C1]], 8

; CHECK-NEXT: %8 = inttoptr i32 %[[M3]] to i32*
; CHECK-NEXT: %9 = load volatile i32, i32* %8, align 4
; CHECK-NEXT: %[[M4:const_mat[0-9]?]] = add i32 %[[C1]], 12
; CHECK-NEXT: %10 = inttoptr i32 %[[M4]] to i32*
; CHECK-NEXT: %11 = load volatile i32, i32* %10, align 4

define void @foo_i32() {
entry:
 %0 = load volatile i32, i32* inttoptr (i32 805874688 to i32*), align 4
 %1 = load volatile i32, i32* inttoptr (i32 805874692 to i32*), align 4
 %2 = load volatile i32, i32* inttoptr (i32 805874812 to i32*), align 4
 %3 = load volatile i32, i32* inttoptr (i32 805874816 to i32*), align 4
 %4 = load volatile i32, i32* inttoptr (i32 805874824 to i32*), align 4
 %5 = load volatile i32, i32* inttoptr (i32 805874828 to i32*), align 4
 ret void
}

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; RUN: llc < %s -mtriple=x86_64-linux-android -mattr=+mmx -enable-legalize-types-checking | FileCheck %s
;
; D31946
; Check that we dont end up with the ""LLVM ERROR: Cannot select" error.
; Additionally ensure that the output code actually put fp128 values in SSE registers.

declare fp128 @llvm.fabs.f128(fp128)
declare fp128 @llvm.copysign.f128(fp128, fp128)

```
define fp128 @TestSelect(fp128 %a, fp128 %b) {
 %cmp = fcmp ogt fp128 %a, %b
 %sub = fsub fp128 %a, %b
 %res = select i1 %cmp, fp128 %sub, fp128 0xL00000000000000000000000000000000
 ret fp128 %res
; CHECK-LABEL: TestSelect:
; CHECK       movaps 16(%rsp), %xmm1
; CHECK-NEXT   callq __subtf3
; CHECK-NEXT   testl %ebx, %ebx
; CHECK-NEXT   jg .LBB0_2
; CHECK-NEXT # %bb.1:
; CHECK-NEXT   movaps .LCPI0_0(%rip), %xmm0
; CHECK-NEXT .LBB0_2:
; CHECK-NEXT   addq $32, %rsp
; CHECK-NEXT   popq %rbx
; CHECK-NEXT   retq
}

define fp128 @TestFabs(fp128 %a) {
 %res = call fp128 @llvm.fabs.f128(fp128 %a)
 ret fp128 %res
; CHECK-LABEL: TestFabs:
; CHECK      andps .LCPI1_0(%rip), %xmm0
; CHECK-NEXT retq
}

define fp128 @TestCopysign(fp128 %a, fp128 %b) {
 %res = call fp128 @llvm.copysign.f128(fp128 %a, fp128 %b)
 ret fp128 %res
; CHECK-LABEL: TestCopysign:
; CHECK      andps .LCPI2_1(%rip), %xmm0
; CHECK-NEXT orps %xmm1, %xmm0
; CHECK-NEXT retq
}

define fp128 @TestFneg(fp128 %a) {
 %mul = fmul fp128 %a, %a
 %res = fsub fp128 0xL00000000000000008000000000000000, %mul
 ret fp128 %res
; CHECK-LABEL: TestFneg:
; CHECK      movaps %xmm0, %xmm1
; CHECK-NEXT callq __multf3
; CHECK-NEXT xorps .LCPI3_0(%rip), %xmm0
; CHECK-NEXT popq %rax
; CHECK-NEXT retq
}
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```

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jar/com/squareup/okhttp/ConnectionSpec.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/Callback.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/ResponseBody.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/framed/PushObserver.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/Credentials.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/RequestBody.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/Version.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/Challenge.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/Call.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/Interceptor.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/http/CacheRequest.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/http/HttpMethod.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/Protocol.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/TlsVersion.java

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jar/com/squareup/okhttp/internal/io/RealConnection.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/tls/DistinguishedNameParser.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/http/HttpEngine.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/tls/OkHostnameVerifier.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/ConnectionPool.java
* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/Headers.java
* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/OptionalMethod.java
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* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/http/HttpStream.java
* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/Util.java
* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/http/Http1xStream.java
* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/http/Http2xStream.java
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jar/com/squareup/okhttp/internal/framed/FrameReader.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/http/HttpDate.java

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jar/com/squareup/okhttp/internal/framed/Spdy3.java

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jar/com/squareup/okhttp/internal/http/HeaderParser.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/framed/FrameWriter.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/framed/FramedConnection.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/DiskLruCache.java

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* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/Route.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/Response.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/framed/NameValueBlockReader.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-
jar/com/squareup/okhttp/internal/http/AuthenticatorAdapter.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-

jar/com/squareup/okhttp/internal/framed/HeadersMode.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/MediaType.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/internal/NamedRunnable.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/internal/RouteDatabase.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/internal/framed/Http2.java

* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/Request.java

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* /opt/cola/permits/1107950648_1605891205.99/0/okhttp-2-7-0-sources-1-jar/com/squareup/okhttp/internal/framed/Variant.java

1.116 recyclerview 1.1.0-alpha07

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When layoutManager xml attribute is used, RecyclerView inflates
#LayoutManagers' constructors using reflection.
-keep public class * extends androidx.recyclerview.widget.RecyclerView$LayoutManager {
  public <init>(android.content.Context, android.util.AttributeSet, int, int);
  public <init>();
}

-keepclassmembers class androidx.recyclerview.widget.RecyclerView {
  public void suppressLayout(boolean);
  public boolean isLayoutSuppressed();
}

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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/res/layout/autofill_rv.xml
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*/
/**
  * A ViewHolder describes an item view and metadata about its place within the RecyclerView.
  *
  * <p>{@link Adapter} implementations should subclass ViewHolder and add fields for caching

* potentially expensive {@link View#findViewById(int)} results.</p>
 *
 * <p>While {@link LayoutParams} belong to the {@link LayoutManager},
 * {@link ViewHolder ViewHolders} belong to the adapter. Adapters should feel free to use
 * their own custom ViewHolder implementations to store data that makes binding view contents
 * easier. Implementations should assume that individual item views will hold strong references
 * to <code>ViewHolder</code> objects and that <code>RecyclerView</code> instances may hold
 * strong references to extra off-screen item views for caching purposes</p>
 */

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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/main/java/androidx/recyclerview/widget/RecyclerView.java
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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/res/drawable/fast_scroll_track_drawable.xml
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/res/drawable/fast_scroll_thumb_drawable.xml
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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/main/java/androidx/recyclerview/selection/AutoScroller.java
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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/androidTest/java/androidx/recyclerview/selection/TouchInputHandlerTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/androidTest/java/androidx/recyclerview/selection/testing/TestHolder.java
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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/androidTest/java/androidx/recyclerview/selection/MouseInputHandlerTest.java
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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/main/java/androidx/recyclerview/selection/BandSelectionHelper.java
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gz/recyclerview/src/main/java/androidx/recyclerview/widget/StaggeredGridLayoutManager.java

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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/RecyclerViewNestedScrollingFlingTest.kt

* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/PagerSnapHelperCenterTest.kt

* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/RecyclerViewNestedScrollingSmoothScrollBy Test.java

* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/androidTest/java/androidx/recyclerview/selection/ResetMangerTest.java

* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/BaseSnapHelperCenterTest.kt

* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/androidTest/java/androidx/recyclerview/selection/GestureDetectorWrapperTest.java

* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/main/java/androidx/recyclerview/selection/GestureDetectorWrapper.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/main/java/androidx/recyclerview/selection/ResetManager.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/LinearSnapHelperCenterTest.kt
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/RecyclerViewNestedScrolling3RequestDisallowInterceptTouchTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/androidTest/java/androidx/recyclerview/selection/testing/TestDragListener.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/RecyclerViewNestedScrollingMouseScrollTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/LinearLayoutManagerExtraLayoutSpaceTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/main/java/androidx/recyclerview/selection/StubOnItemTouchListener.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/RecyclerViewNestedScrollingScrollByTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/LinearSmoothScrollerTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/androidTest/java/androidx/recyclerview/selection/ToolHandlerRegistryTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/androidTest/java/androidx/recyclerview/selection/testing/TestResettable.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/main/java/androidx/recyclerview/selection/Resettable.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/androidTest/java/androidx/recyclerview/selection/SelectionTrackerTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/LazyStateRestorationTest.kt
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/androidTest/java/androidx/recyclerview/selection/StableIdKeyProviderTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/RecyclerViewNestedScrollingA11yScrollTest.java
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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/res/values/ids.xml
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/res/values/attrs.xml
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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-benchmark/src/main/AndroidManifest.xml
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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-
gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/ConcatAdapterSubject.kt
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-
selection/src/androidTest/java/androidx/recyclerview/selection/EventBackstopTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-
lint/src/main/java/androidx/recyclerview/lint/InvalidSetHasFixedSizeDetector.kt
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-
selection/src/androidTest/java/androidx/recyclerview/selection/testing/TestOnItemTouchListener.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-
lint/src/test/java/androidx/recyclerview/lint/Stubs.kt
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-
selection/src/androidTest/java/androidx/recyclerview/selection/EventRouterTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-
selection/src/androidTest/java/androidx/recyclerview/selection/DisallowInterceptFilterTest.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-
lint/src/main/java/androidx/recyclerview/lint/RecyclerViewIssueRegistry.kt
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-
benchmark/src/androidTest/java/androidx/recyclerview/benchmark/DiffBenchmark.kt
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-
gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/LinearLayoutManagerRemoveShownItemsTest.
kt
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-
gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/LinearLayoutManagerFindReferenceChildTest.
kt
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-
gz/recyclerview/src/main/java/androidx/recyclerview/widget/StableIdStorage.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-
gz/recyclerview/src/main/java/androidx/recyclerview/widget/ConcatAdapterController.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-
lint/build.gradle
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-
lint/src/test/java/androidx/recyclerview/lint/InvalidSetHasFixedSizeTest.kt
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-
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* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-
gz/recyclerview/src/main/java/androidx/recyclerview/widget/NestedAdapterWrapper.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-
gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/ConcatAdapterTest.kt
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-
selection/src/main/java/androidx/recyclerview/selection/EventBackstop.java
* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-
gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/LinearLayoutManagerFindZeroPxReferenceChi
ldTest.kt

* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/main/java/androidx/recyclerview/widget/ConcatAdapter.java

* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/main/java/androidx/recyclerview/widget/ViewTypeStorage.java

* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview-selection/src/main/java/androidx/recyclerview/selection/DisallowInterceptFilter.java

* /opt/cola/permits/1205110155_1637344547.82/0/support-androidx-main-recyclerview-tar-gz/recyclerview/src/androidTest/java/androidx/recyclerview/widget/RecyclerListenerTest.java

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-*-makefile-*-

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BSD-specific setup (FreeBSD, OpenBSD, NetBSD, *BSD)

```
## Copyright (c) 1999-2013, International Business Machines Corporation and
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## Commands to generate dependency files
GEN_DEPS.c= $(CC) -E -MM $(DEFS) $(CPPFLAGS)
GEN_DEPS.cc= $(CXX) -E -MM $(DEFS) $(CPPFLAGS)

## Flags for position independent code
SHAREDLIBCFLAGS = -fPIC
SHAREDLIBCXXFLAGS = -fPIC
SHAREDLIBCPPFLAGS = -DPIC

## Additional flags when building libraries and with threads
THREADSCPPFLAGS = -D_REENTRANT
LIBCPPFLAGS =

## Compiler switch to embed a runtime search path
LD_RPATH=
LD_RPATH_PRE= -Wl,-rpath,

## Compiler switch to embed a library name
LD_SONAME = -Wl,-soname -Wl,$(notdir $(MIDDLE_SO_TARGET))

## Shared library options
LD_SOOPTIONS= -Wl,-Bsymbolic

## Shared object suffix
SO = so
## Non-shared intermediate object suffix
STATIC_O = ao

## Compilation rules
%.$(STATIC_O): $(srcdir)/%.c
 $(COMPILE.c) $(STATICCPPFLAGS) $(STATICCFLAGS) -o $@ $<
%.o: $(srcdir)/%.c
 $(COMPILE.c) $(DYNAMICCPPFLAGS) $(DYNAMICCFLAGS) -o $@ $<

%.$(STATIC_O): $(srcdir)/%.cpp
 $(COMPILE.cc) $(STATICCPPFLAGS) $(STATICCXXFLAGS) -o $@ $<
%.o: $(srcdir)/%.cpp
 $(COMPILE.cc) $(DYNAMICCPPFLAGS) $(DYNAMICCXXFLAGS) -o $@ $<


## Dependency rules
%.d: $(srcdir)/%.c
 @echo "generating dependency information for $<"
 @$(SHELL) -ec '$(GEN_DEPS.c) $< \
 | sed '\"s/\($*\)\.o[ :]*/\1.o $@ : /g'\" > $@; \
```

```
    [ -s $@ ] || rm -f $@'

%.d: $(srcdir)/%.cpp
 @echo "generating dependency information for $<"
 @$(SHELL) -ec '$(GEN_DEPS.cc) $< \
 | sed '\"s/\($*\)\.o[ :]*/\1.o $@ : /g'\" > $@; \
 [ -s $@ ] || rm -f $@'

## Versioned libraries rules

%.$(SO).$(SO_TARGET_VERSION_MAJOR): %.$(SO).$(SO_TARGET_VERSION)
 $(RM) $@ && ln -s ${<F} $@
%.$(SO): %.$(SO).$(SO_TARGET_VERSION_MAJOR)
 $(RM) $@ && ln -s ${*F}.$(SO).$(SO_TARGET_VERSION) $@

##  Bind internal references

# LDflags that pkgdata will use
BIR_LDFLAGS= -Wl,-Bsymbolic

# Dependencies [i.e. map files] for the final library
BIR_DEPS=

## Remove shared library 's'
STATIC_PREFIX_WHEN_USED =
STATIC_PREFIX =

## End BSD-specific setup
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1.120 util-linux 2.24

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jar/com/google/gson/stream/MalformedJsonException.java
* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-
jar/com/google/gson/stream/JsonScope.java
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jar/com/google/gson/annotations/Until.java
* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-jar/com/google/gson/GsonBuilder.java
* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-
jar/com/google/gson/JsonDeserializationContext.java
* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-jar/com/google/gson/JsonElement.java
* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-
jar/com/google/gson/JsonIOException.java
* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-jar/com/google/gson/JsonDeserializer.java
* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-
jar/com/google/gson/FieldNamingStrategy.java
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jar/com/google/gson/internal/ObjectConstructor.java
* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-
jar/com/google/gson/annotations/SerializedName.java
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jar/com/google/gson/JsonSerializationContext.java
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jar/com/google/gson/annotations/Since.java
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jar/com/google/gson/DefaultDateTypeAdapter.java
* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-

jar/com/google/gson/reflect/TypeToken.java

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jar/com/google/gson/FieldNamingPolicy.java

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jar/com/google/gson/annotations/Expose.java

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* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-
jar/com/google/gson/ExclusionStrategy.java

* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-jar/com/google/gson/JsonPrimitive.java

* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-jar/com/google/gson/InstanceCreator.java

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jar/com/google/gson/internal/$Gson$Preconditions.java

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jar/com/google/gson/JsonParseException.java

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* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-
jar/com/google/gson/TypeAdapterFactory.java
* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-
jar/com/google/gson/internal/bind/ArrayTypeAdapter.java
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jar/com/google/gson/internal/bind/CollectionTypeAdapterFactory.java
* /opt/cola/permits/1001166424_1608115822.07/0/gson-2-3-1-sources-2-
jar/com/google/gson/internal/bind/ReflectiveTypeAdapterFactory.java

1.125 sqlite 3.22.0

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Jean-loup Gailly   Mark Adler
jloup@gzip.org   madler@alumni.caltech.edu

The data format used by the zlib library is described by RFCs (Request for
Comments) 1950 to 1952 in the files http://tools.ietf.org/html/rfc1950
(zlib format), rfc1951 (deflate format) and rfc1952 (gzip format).
*/

1.128 toybox 0.7.3-6.ph2
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1.129 cups 2.2.9

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possible use to the public, the best way to achieve this is to make it
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To do so, attach the following notices to the program. It is safest
to attach them to the start of each source file to most effectively
convey the exclusion of warranty; and each file should have at least
the "copyright" line and a pointer to where the full notice is found.

    <one line to give the program's name and a brief idea of what it does.>
    Copyright (C) 19yy <name of author>

    This program is free software; you can redistribute it and/or modify
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Foundation, Inc., 675 Mass Ave, Cambridge, MA 02139, USA.

Also add information on how to contact you by electronic and paper mail.

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when it starts in an interactive mode:

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    This is free software, and you are welcome to redistribute it
    under certain conditions; type `show c' for details.

The hypothetical commands `show w' and `show c' should show the appropriate
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school, if any, to sign a "copyright disclaimer" for the program, if
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 `Gnomovision' (which makes passes at compilers) written by James Hacker.

 <signature of Ty Coon>, 1 April 1989
 Ty Coon, President of Vice

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 [This is the first released version of the library GPL. It is
 numbered 2 because it goes with version 2 of the ordinary GPL.]

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 The reason we have a separate public license for some libraries is that
they blur the distinction we usually make between modifying or adding to a
program and simply using it. Linking a program with a library, without
changing the library, is in some sense simply using the library, and is
analogous to running a utility program or application program. However, in
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treats it as such.

 Because of this blurred distinction, using the ordinary General
Public License for libraries did not effectively promote software
sharing, because most developers did not use the libraries. We
concluded that weaker conditions might promote sharing better.

 However, unrestricted linking of non-free programs would deprive the
users of those programs of all benefit from the free status of the
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preserving your freedom as a user of such programs to change the free
libraries that are incorporated in them. (We have not seen how to achieve
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will lead to faster development of free libraries.

 The precise terms and conditions for copying, distribution and
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is invoked, then you must make a good faith effort to ensure that,
in the event an application does not supply such function or
table, the facility still operates, and performs whatever part of
its purpose remains meaningful.

(For example, a function in a library to compute square roots has
a purpose that is entirely well-defined independent of the
application. Therefore, Subsection 2d requires that any
application-supplied function or table used by this function must
be optional: if the application does not supply it, the square
root function must still compute square roots.)

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subsequent copies and derivative works made from that copy.

This option is useful when you wish to copy part of the code of
the Library into a program that is not a library.

4. You may copy and distribute the Library (or a portion or
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under the terms of Sections 1 and 2 above provided that you accompany
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must be distributed under the terms of Sections 1 and 2 above on a
medium customarily used for software interchange.

If distribution of object code is made by offering access to copy
from a designated place, then offering equivalent access to copy the
source code from the same place satisfies the requirement to
distribute the source code, even though third parties are not
compelled to copy the source along with the object code.

5. A program that contains no derivative of any portion of the
Library, but is designed to work with the Library by being compiled or
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However, linking a "work that uses the Library" with the Library
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library". The executable is therefore covered by this License.
Section 6 states terms for distribution of such executables.

When a "work that uses the Library" uses material from a header file
that is part of the Library, the object code for the work may be a
derivative work of the Library even though the source code is not.
Whether this is true is especially significant if the work can be
linked without the Library, or if the work is itself a library. The
threshold for this to be true is not precisely defined by law.

If such an object file uses only numerical parameters, data
structure layouts and accessors, and small macros and small inline
functions (ten lines or less in length), then the use of the object
file is unrestricted, regardless of whether it is legally a derivative
work. (Executables containing this object code plus portions of the
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Otherwise, if the work is a derivative of the Library, you may
distribute the object code for the work under the terms of Section 6.

Any executables containing that work also fall under Section 6, whether or not they are linked directly with the Library itself.

 6. As an exception to the Sections above, you may also compile or link a "work that uses the Library" with the Library to produce a work containing portions of the Library, and distribute that work under terms of your choice, provided that the terms permit modification of the work for the customer's own use and reverse engineering for debugging such modifications.

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  changes were used in the work (which must be distributed under
  Sections 1 and 2 above); and, if the work is an executable linked
  with the Library, with the complete machine-readable "work that
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  specified in Subsection 6a, above, for a charge no more
  than the cost of performing this distribution.

  c) If distribution of the work is made by offering access to copy
  from a designated place, offer equivalent access to copy the above
  specified materials from the same place.

  d) Verify that the user has already received a copy of these
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b) Give prominent notice with the combined library of the fact
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   Appendix: How to Apply These Terms to Your New Libraries

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redistribution under these terms (or, alternatively, under the terms of the
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To apply these terms, attach the following notices to the library. It is
safest to attach them to the start of each source file to most effectively
convey the exclusion of warranty; and each file should have at least the
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<one line to give the library's name and a brief idea of what it does.>
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That's all there is to it!

1.130 opencore-amr 1.1.1

1.130.1 Available under license :

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* snprintf.c - a portable implementation of snprintf

*

* AUTHOR

*   Mark Martinec <mark.martinec@ijs.si>, April 1999.

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1.137 lcms 2.8

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1.139 libvorbis 0.4.5

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1.146 icu 63

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## Commands to generate dependency files
GEN_DEPS.c= $(CC) -E -MM $(DEFS) $(CPPFLAGS)
GEN_DEPS.cc= $(CXX) -E -MM $(DEFS) $(CPPFLAGS)

## Flags for position independent code
SHAREDLIBCFLAGS = -fPIC
SHAREDLIBCXXFLAGS = -fPIC
SHAREDLIBCPPFLAGS = -DPIC

## Additional flags when building libraries and with threads
THREADSCPPFLAGS = -D_REENTRANT
LIBCPPFLAGS =

## Compiler switch to embed a runtime search path
LD_RPATH=
LD_RPATH_PRE= -Wl,-rpath,

## Compiler switch to embed a library name
LD_SONAME = -Wl,-soname -Wl,$(notdir $(MIDDLE_SO_TARGET))

## Shared library options
LD_SOOPTIONS= -Wl,-Bsymbolic

## Shared object suffix
SO = so
## Non-shared intermediate object suffix
STATIC_O = ao

## Compilation rules
%.$(STATIC_O): $(srcdir)/%.c
 $(COMPILE.c) $(STATICCPPFLAGS) $(STATICCFLAGS) -o $@ $<
%.o: $(srcdir)/%.c
 $(COMPILE.c) $(DYNAMICCPPFLAGS) $(DYNAMICCFLAGS) -o $@ $<
```

```
%.$(STATIC_O): $(srcdir)/%.cpp
 $(COMPILE.cc) $(STATICCPPFLAGS) $(STATICCXXFLAGS) -o $@ $<
%.o: $(srcdir)/%.cpp
 $(COMPILE.cc) $(DYNAMICCPPFLAGS) $(DYNAMICCXXFLAGS) -o $@ $<


## Dependency rules
%.d: $(srcdir)/%.c
 @echo "generating dependency information for $<"
 @$(SHELL) -ec '$(GEN_DEPS.c) $< \
 | sed '\"s/\($*\)\.o[ :]*/\1.o $@ : /g'\" > $@; \
 [ -s $@ ] || rm -f $@'

%.d: $(srcdir)/%.cpp
 @echo "generating dependency information for $<"
 @$(SHELL) -ec '$(GEN_DEPS.cc) $< \
 | sed '\"s/\($*\)\.o[ :]*/\1.o $@ : /g'\" > $@; \
 [ -s $@ ] || rm -f $@'

## Versioned libraries rules

%.$(SO).$(SO_TARGET_VERSION_MAJOR): %.$(SO).$(SO_TARGET_VERSION)
 $(RM) $@ && ln -s ${<F} $@
%.$(SO): %.$(SO).$(SO_TARGET_VERSION_MAJOR)
 $(RM) $@ && ln -s ${*F}.$(SO).$(SO_TARGET_VERSION) $@

##  Bind internal references

# LDflags that pkgdata will use
BIR_LDFLAGS= -Wl,-Bsymbolic

# Dependencies [i.e. map files] for the final library
BIR_DEPS=

## Remove shared library 's'
STATIC_PREFIX_WHEN_USED =
STATIC_PREFIX =

## End BSD-specific setup
```

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1.149 libjpeg 6b

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1.149.2 Available under license :

The Independent JPEG Group's JPEG software
==

README for release 6b of 27-Mar-1998
====================================

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larger programs) should contact IJG at jpeg-info@uunet.uu.net to be added to
our electronic mailing list. Mailing list members are notified of updates
and have a chance to participate in technical discussions, etc.

This software is the work of Tom Lane, Philip Gladstone, Jim Boucher,
Lee Crocker, Julian Minguillon, Luis Ortiz, George Phillips, Davide Rossi,
Guido Vollbeding, Ge' Weijers, and other members of the Independent JPEG
Group.

IJG is not affiliated with the official ISO JPEG standards committee.

DOCUMENTATION ROADMAP
=====================

This file contains the following sections:

OVERVIEW   General description of JPEG and the IJG software.
LEGAL ISSUES   Copyright, lack of warranty, terms of distribution.
REFERENCES   Where to learn more about JPEG.
ARCHIVE LOCATIONS   Where to find newer versions of this software.
RELATED SOFTWARE   Other stuff you should get.
FILE FORMAT WARS   Software *not* to get.
TO DO   Plans for future IJG releases.

Other documentation files in the distribution are:

User documentation:
 install.doc   How to configure and install the IJG software.
 usage.doc   Usage instructions for cjpeg, djpeg, jpegtran,

rdjpgcom, and wrjpgcom.

*.1   Unix-style man pages for programs (same info as usage.doc).

wizard.doc   Advanced usage instructions for JPEG wizards only.

change.log   Version-to-version change highlights.

Programmer and internal documentation:

libjpeg.doc   How to use the JPEG library in your own programs.

example.c   Sample code for calling the JPEG library.

structure.doc   Overview of the JPEG library's internal structure.

filelist.doc   Road map of IJG files.

coderules.doc   Coding style rules --- please read if you contribute code.

Please read at least the files install.doc and usage.doc. Useful information
can also be found in the JPEG FAQ (Frequently Asked Questions) article. See
ARCHIVE LOCATIONS below to find out where to obtain the FAQ article.

If you want to understand how the JPEG code works, we suggest reading one or
more of the REFERENCES, then looking at the documentation files (in roughly
the order listed) before diving into the code.

OVERVIEW
========

This package contains C software to implement JPEG image compression and
decompression. JPEG (pronounced "jay-peg") is a standardized compression
method for full-color and gray-scale images. JPEG is intended for compressing
"real-world" scenes; line drawings, cartoons and other non-realistic images
are not its strong suit. JPEG is lossy, meaning that the output image is not
exactly identical to the input image. Hence you must not use JPEG if you
have to have identical output bits. However, on typical photographic images,
very good compression levels can be obtained with no visible change, and
remarkably high compression levels are possible if you can tolerate a
low-quality image. For more details, see the references, or just experiment
with various compression settings.

This software implements JPEG baseline, extended-sequential, and progressive
compression processes. Provision is made for supporting all variants of these
processes, although some uncommon parameter settings aren't implemented yet.
For legal reasons, we are not distributing code for the arithmetic-coding
variants of JPEG; see LEGAL ISSUES. We have made no provision for supporting
the hierarchical or lossless processes defined in the standard.

We provide a set of library routines for reading and writing JPEG image files,
plus two sample applications "cjpeg" and "djpeg", which use the library to
perform conversion between JPEG and some other popular image file formats.
The library is intended to be reused in other applications.

In order to support file conversion and viewing software, we have included

considerable functionality beyond the bare JPEG coding/decoding capability;
for example, the color quantization modules are not strictly part of JPEG
decoding, but they are essential for output to colormapped file formats or
colormapped displays. These extra functions can be compiled out of the
library if not required for a particular application. We have also included
"jpegtran", a utility for lossless transcoding between different JPEG
processes, and "rdjpgcom" and "wrjpgcom", two simple applications for
inserting and extracting textual comments in JFIF files.

The emphasis in designing this software has been on achieving portability and
flexibility, while also making it fast enough to be useful. In particular,
the software is not intended to be read as a tutorial on JPEG. (See the
REFERENCES section for introductory material.) Rather, it is intended to
be reliable, portable, industrial-strength code. We do not claim to have
achieved that goal in every aspect of the software, but we strive for it.

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that you must include source code if you redistribute it. (See the file
ansi2knr.c for full details.) However, since ansi2knr.c is not needed as part
of any program generated from the IJG code, this does not limit you more than
the foregoing paragraphs do.

The Unix configuration script "configure" was produced with GNU Autoconf.
It is copyright by the Free Software Foundation but is freely distributable.
The same holds for its supporting scripts (config.guess, config.sub,
ltconfig, ltmain.sh). Another support script, install-sh, is copyright
by M.I.T. but is also freely distributable.

It appears that the arithmetic coding option of the JPEG spec is covered by
patents owned by IBM, AT&T, and Mitsubishi. Hence arithmetic coding cannot
legally be used without obtaining one or more licenses. For this reason,
support for arithmetic coding has been removed from the free JPEG software.
(Since arithmetic coding provides only a marginal gain over the unpatented
Huffman mode, it is unlikely that very many implementations will support it.)
So far as we are aware, there are no patent restrictions on the remaining
code.

The IJG distribution formerly included code to read and write GIF files.

To avoid entanglement with the Unisys LZW patent, GIF reading support has
been removed altogether, and the GIF writer has been simplified to produce
"uncompressed GIFs". This technique does not use the LZW algorithm; the
resulting GIF files are larger than usual, but are readable by all standard
GIF decoders.

We are required to state that
   "The Graphics Interchange Format(c) is the Copyright property of
   CompuServe Incorporated. GIF(sm) is a Service Mark property of
   CompuServe Incorporated."

REFERENCES

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We highly recommend reading one or more of these references before trying to
understand the innards of the JPEG software.

The best short technical introduction to the JPEG compression algorithm is
 Wallace, Gregory K. "The JPEG Still Picture Compression Standard",
 Communications of the ACM, April 1991 (vol. 34 no. 4), pp. 30-44.
(Adjacent articles in that issue discuss MPEG motion picture compression,
applications of JPEG, and related topics.) If you don't have the CACM issue
handy, a PostScript file containing a revised version of Wallace's article is
available at ftp://ftp.uu.net/graphics/jpeg/wallace.ps.gz. The file (actually
a preprint for an article that appeared in IEEE Trans. Consumer Electronics)
omits the sample images that appeared in CACM, but it includes corrections
and some added material. Note: the Wallace article is copyright ACM and IEEE,
and it may not be used for commercial purposes.

A somewhat less technical, more leisurely introduction to JPEG can be found in
"The Data Compression Book" by Mark Nelson and Jean-loup Gailly, published by
M&T Books (New York), 2nd ed. 1996, ISBN 1-55851-434-1. This book provides
good explanations and example C code for a multitude of compression methods
including JPEG. It is an excellent source if you are comfortable reading C
code but don't know much about data compression in general. The book's JPEG
sample code is far from industrial-strength, but when you are ready to look
at a full implementation, you've got one here...

The best full description of JPEG is the textbook "JPEG Still Image Data
Compression Standard" by William B. Pennebaker and Joan L. Mitchell, published
by Van Nostrand Reinhold, 1993, ISBN 0-442-01272-1. Price US$59.95, 638 pp.
The book includes the complete text of the ISO JPEG standards (DIS 10918-1
and draft DIS 10918-2). This is by far the most complete exposition of JPEG
in existence, and we highly recommend it.

The JPEG standard itself is not available electronically; you must order a
paper copy through ISO or ITU. (Unless you feel a need to own a certified

official copy, we recommend buying the Pennebaker and Mitchell book instead; it's much cheaper and includes a great deal of useful explanatory material.) In the USA, copies of the standard may be ordered from ANSI Sales at (212) 642-4900, or from Global Engineering Documents at (800) 854-7179. (ANSI doesn't take credit card orders, but Global does.) It's not cheap: as of 1992, ANSI was charging $95 for Part 1 and $47 for Part 2, plus 7% shipping/handling. The standard is divided into two parts, Part 1 being the actual specification, while Part 2 covers compliance testing methods. Part 1 is titled "Digital Compression and Coding of Continuous-tone Still Images, Part 1: Requirements and guidelines" and has document numbers ISO/IEC IS 10918-1, ITU-T T.81. Part 2 is titled "Digital Compression and Coding of Continuous-tone Still Images, Part 2: Compliance testing" and has document numbers ISO/IEC IS 10918-2, ITU-T T.83.

Some extensions to the original JPEG standard are defined in JPEG Part 3, a newer ISO standard numbered ISO/IEC IS 10918-3 and ITU-T T.84. IJG currently does not support any Part 3 extensions.

The JPEG standard does not specify all details of an interchangeable file format. For the omitted details we follow the "JFIF" conventions, revision 1.02. A copy of the JFIF spec is available from:
 Literature Department
 C-Cube Microsystems, Inc.
 1778 McCarthy Blvd.
 Milpitas, CA 95035
 phone (408) 944-6300, fax (408) 944-6314
A PostScript version of this document is available by FTP at ftp://ftp.uu.net/graphics/jpeg/jfif.ps.gz. There is also a plain text version at ftp://ftp.uu.net/graphics/jpeg/jfif.txt.gz, but it is missing the figures.

The TIFF 6.0 file format specification can be obtained by FTP from ftp://ftp.sgi.com/graphics/tiff/TIFF6.ps.gz. The JPEG incorporation scheme found in the TIFF 6.0 spec of 3-June-92 has a number of serious problems. IJG does not recommend use of the TIFF 6.0 design (TIFF Compression tag 6). Instead, we recommend the JPEG design proposed by TIFF Technical Note #2 (Compression tag 7). Copies of this Note can be obtained from ftp.sgi.com or from ftp://ftp.uu.net/graphics/jpeg/. It is expected that the next revision of the TIFF spec will replace the 6.0 JPEG design with the Note's design. Although IJG's own code does not support TIFF/JPEG, the free libtiff library uses our library to implement TIFF/JPEG per the Note. libtiff is available from ftp://ftp.sgi.com/graphics/tiff/.

ARCHIVE LOCATIONS
=================

The "official" archive site for this software is ftp.uu.net (Internet

address 192.48.96.9). The most recent released version can always be found
there in directory graphics/jpeg. This particular version will be archived
as ftp://ftp.uu.net/graphics/jpeg/jpegsrc.v6b.tar.gz. If you don't have
direct Internet access, UUNET's archives are also available via UUCP; contact
help@uunet.uu.net for information on retrieving files that way.

Numerous Internet sites maintain copies of the UUNET files. However, only
ftp.uu.net is guaranteed to have the latest official version.

You can also obtain this software in DOS-compatible "zip" archive format from
the SimTel archives (ftp://ftp.simtel.net/pub/simtelnet/msdos/graphics/), or
on CompuServe in the Graphics Support forum (GO CIS:GRAPHSUP), library 12
"JPEG Tools". Again, these versions may sometimes lag behind the ftp.uu.net
release.

The JPEG FAQ (Frequently Asked Questions) article is a useful source of
general information about JPEG. It is updated constantly and therefore is
not included in this distribution. The FAQ is posted every two weeks to
Usenet newsgroups comp.graphics.misc, news.answers, and other groups.
It is available on the World Wide Web at http://www.faqs.org/faqs/jpeg-faq/
and other news.answers archive sites, including the official news.answers
archive at rtfm.mit.edu: ftp://rtfm.mit.edu/pub/usenet/news.answers/jpeg-faq/.
If you don't have Web or FTP access, send e-mail to mail-server@rtfm.mit.edu
with body
 send usenet/news.answers/jpeg-faq/part1
 send usenet/news.answers/jpeg-faq/part2

RELATED SOFTWARE
================

Numerous viewing and image manipulation programs now support JPEG. (Quite a
few of them use this library to do so.) The JPEG FAQ described above lists
some of the more popular free and shareware viewers, and tells where to
obtain them on Internet.

If you are on a Unix machine, we highly recommend Jef Poskanzer's free
PBMPLUS software, which provides many useful operations on PPM-format image
files. In particular, it can convert PPM images to and from a wide range of
other formats, thus making cjpeg/djpeg considerably more useful. The latest
version is distributed by the NetPBM group, and is available from numerous
sites, notably ftp://wuarchive.wustl.edu/graphics/graphics/packages/NetPBM/.
Unfortunately PBMPLUS/NETPBM is not nearly as portable as the IJG software is;
you are likely to have difficulty making it work on any non-Unix machine.

A different free JPEG implementation, written by the PVRG group at Stanford,
is available from ftp://havefun.stanford.edu/pub/jpeg/. This program
is designed for research and experimentation rather than production use;

it is slower, harder to use, and less portable than the IJG code, but it
is easier to read and modify. Also, the PVRG code supports lossless JPEG,
which we do not. (On the other hand, it doesn't do progressive JPEG.)

FILE FORMAT WARS
================

Some JPEG programs produce files that are not compatible with our library.
The root of the problem is that the ISO JPEG committee failed to specify a
concrete file format. Some vendors "filled in the blanks" on their own,
creating proprietary formats that no one else could read. (For example, none
of the early commercial JPEG implementations for the Macintosh were able to
exchange compressed files.)

The file format we have adopted is called JFIF (see REFERENCES). This format
has been agreed to by a number of major commercial JPEG vendors, and it has
become the de facto standard. JFIF is a minimal or "low end" representation.
We recommend the use of TIFF/JPEG (TIFF revision 6.0 as modified by TIFF
Technical Note #2) for "high end" applications that need to record a lot of
additional data about an image. TIFF/JPEG is fairly new and not yet widely
supported, unfortunately.

The upcoming JPEG Part 3 standard defines a file format called SPIFF.
SPIFF is interoperable with JFIF, in the sense that most JFIF decoders should
be able to read the most common variant of SPIFF. SPIFF has some technical
advantages over JFIF, but its major claim to fame is simply that it is an
official standard rather than an informal one. At this point it is unclear
whether SPIFF will supersede JFIF or whether JFIF will remain the de-facto
standard. IJG intends to support SPIFF once the standard is frozen, but we
have not decided whether it should become our default output format or not.
(In any case, our decoder will remain capable of reading JFIF indefinitely.)

Various proprietary file formats incorporating JPEG compression also exist.
We have little or no sympathy for the existence of these formats. Indeed,
one of the original reasons for developing this free software was to help
force convergence on common, open format standards for JPEG files. Don't
use a proprietary file format!

TO DO
=====

The major thrust for v7 will probably be improvement of visual quality.
The current method for scaling the quantization tables is known not to be
very good at low Q values. We also intend to investigate block boundary
smoothing, "poor man's variable quantization", and other means of improving
quality-vs-file-size performance without sacrificing compatibility.

In future versions, we are considering supporting some of the upcoming JPEG

Part 3 extensions --- principally, variable quantization and the SPIFF file

format.

As always, speeding things up is of great interest.

Please send bug reports, offers of help, etc. to jpeg-info@uunet.uu.net.

1.150 openjpeg 2.3.1

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1.151 libnetfilter-conntrack 1.0.6

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1.152 unbound 1.10.0

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1.153 xz 5.2.5

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